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Use of the Monte Carlo Method in Packaging Thermal Calculations

THERMAL FACTS & FAIRY TALES:
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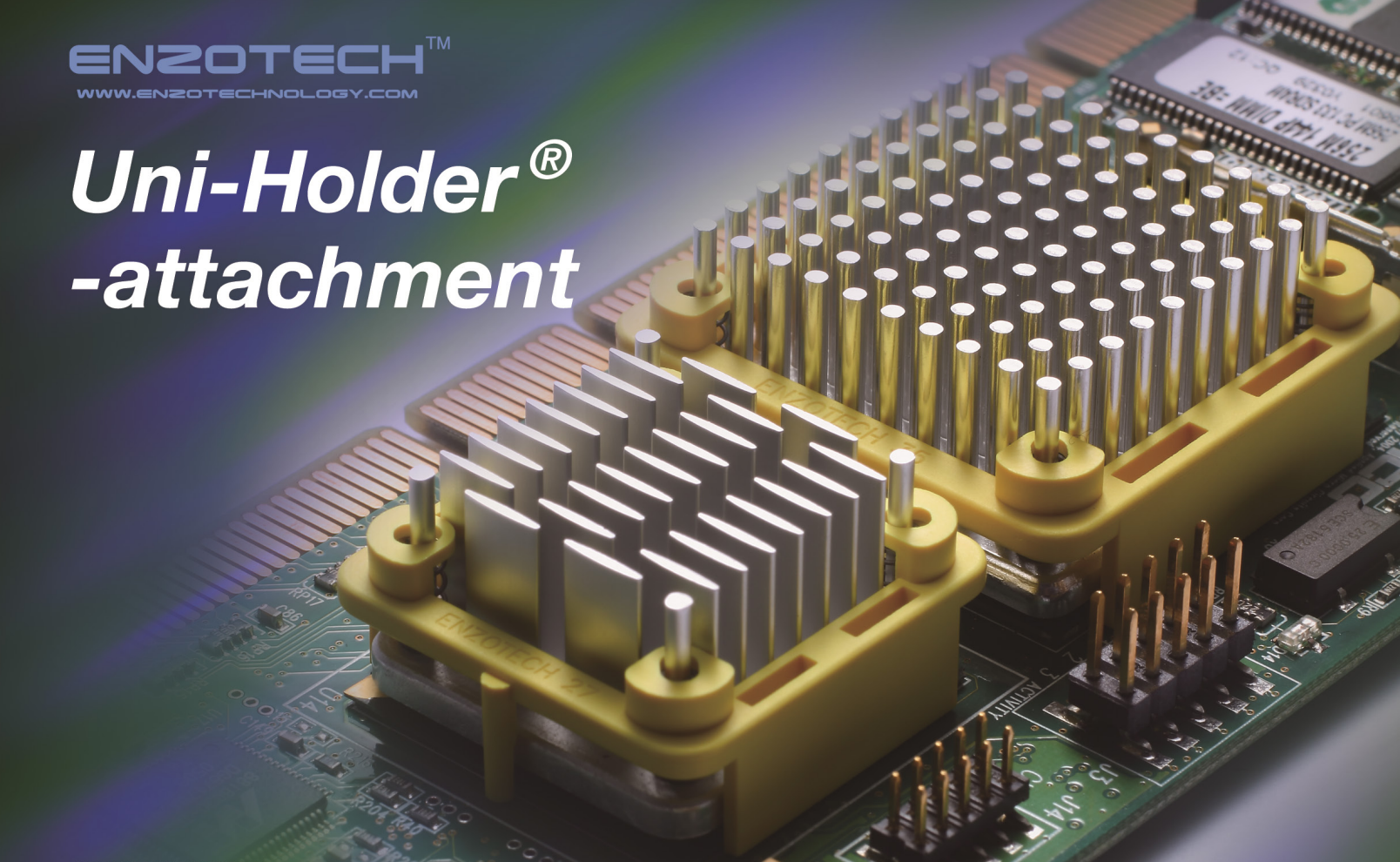
Uni-Holder® -attachment



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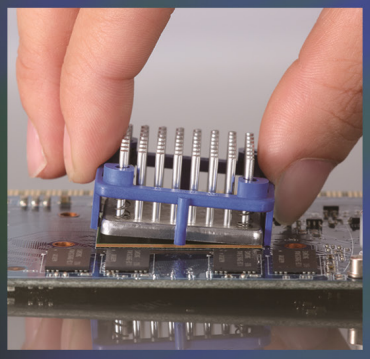
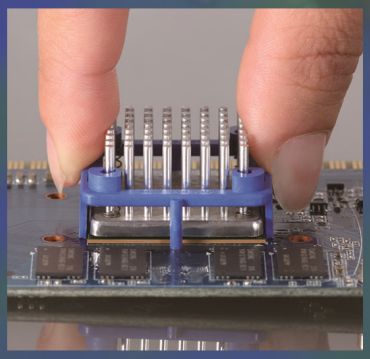


Step 1 :
Center Uni-Holder® on BGA Tilt and hook one side of the clip lip under BGA clip .



Step 2 :
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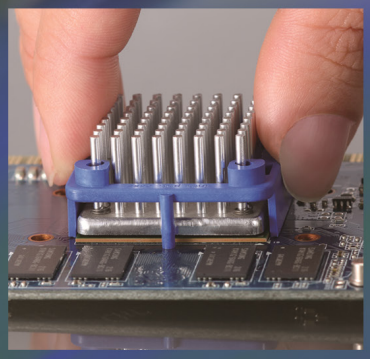
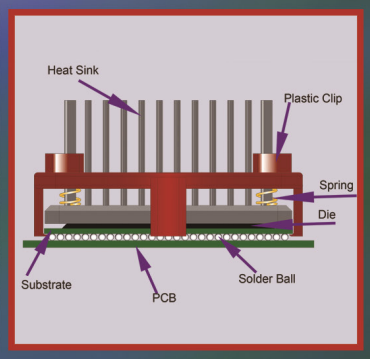


Step 3 :
Installation completed. Snap on . Stay on .



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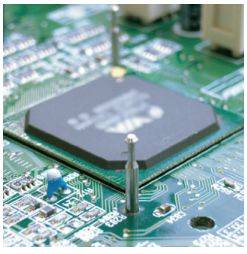

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ITEM MEDIA

EDITORIAL

Victor Chiriac, PhD
Principal Lead Thermal Technologist
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Dear *Electronics Cooling* (EC) readers,

It has been almost 2 years since one of the *Electronics Cooling* magazine editors invited me to join the editorial board. I was both humbled and excited to be involved in this reputable publication, and I hope that together with the EC team, the readers, the technical writers and contributors we will make the publication a greater success in 2018!

The "New Era of Connectivity" has started and 2018 marks a milestone in the industry transition to the fully connected intelligent world, with people and "things" exchanging data in a seamless fashion. Earlier this month, the Consumer Electronics Show (CES) in Las Vegas, the largest technical event in the world, showcased the significant technology leap happening now.

It is an exciting time to work on thermal engineering problems. According to several keynote speakers at CES, the smartphone is the connectivity hub of the entire "connected" industry. In 2017 alone, over 2.4 billion people used phones over the entire world! With a mobile device revolution happening every 12 years, starting in 1983 with the analog phone, followed in 1995 by the digital feature phone, and in 2007 by the smartphone (and mobile internet), what is next? In 2019 and beyond – what is the next evolution stage of the connected world – the super-intelligent phone or something else related to smart virtual reality devices combining multiple features and enabling the consumer to migrate from the current 2-D displays to 3-D projections?

All these questions and on-going technology developments occurring as we write and read this article make our (engineering) life more interesting. Starting in 2018 we will improve the format of the *Electronics Cooling* magazine to migrate from the traditional "topical" issues (pre-defined quarterly topics and feature articles) to a more flexible format where the "hottest ☺" engineering topics happening in our thermal engineering world will be shared with the community.

Technology is driving global economies, transforming our communities and improving our lives. Technology is part of our daily lives – in the US alone, it is 10% of the GDP! The connectivity eco-system is expanding with the migration to 5G, with fiber-like data speeds (100x larger than 4G speeds), low latency and the ability to support unlimited data. It will fuel new services and technologies such as the Internet of Things, augmented reality, autonomous vehicles and smart cities. It is expected that 20% of the world's population will be 5G connected in the next 5 years… Yet 5G brings new thermal challenges and our community will be part of the solution as the technology moves forward.

Although the average US household has more connected devices than ever before, the consumer tech's share of the US home energy use has dropped 25% since 2010! Helping reduce global emissions – self-driving (autonomous) vehicles are exciting and open many avenues for innovation and the need for cooling/thermal management support! With the boom in the world-wide technologies and the thermal problems associated with it, we hope to open the readership gates to many new topics and encourage each of you – our EC readers – to consider submitting feature (or even mini/sketch) articles on various topics of interest that could benefit our community. Artificial Intelligence, medical (wireless) therapy, smart/connected cities, high tech retail, virtual/augmented reality, autonomous driving are all new technologies requiring dedicated thermal solutions worthwhile exploring and sharing with our readers.

I end up here, wishing all of you a happy, healthy, prosperous and creative new year 2018, and I hope to receive your continued support as we embark on a new EC journey this year!

Victor Chiriac
San Diego, CA

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News of Upcoming Thermal Management Events

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SEMI-THERM is an international forum dedicated to the thermal management and characterization of electronic components and systems. It provides knowledge covering all thermal length scales from IC to facility level. The symposium fosters the exchange of knowledge between thermal engineers, professionals and leading experts from industry as well as the exchange of information on the latest academic and industrial advances in electronics thermal management.
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► semi-therm.org

IEEE ITHERM CONFERENCE 2018

May 29th through June 1st, 2018
Sheraton Hotel & Marina San Diego, CA USA

Sponsored by the IEEE's Electronics Packaging Society (EPS), ITherm 2018 is an international conference for scientific and engineering exploration of thermal, thermomechanical and emerging technology issues associated with electronic devices, packages and systems. The first ITherm Conference was held in 1988, making this the 30th year of the Conference Series. ITherm 2018 will be held along with the 66th Electronic Components and Technology Conference (ECTC 2018 - http://www.ectc.net), a premier electronics packaging conference at the Sheraton Hotel and Marina in San Diego. Joint registrations are available at a discounted rate. In addition to paper presentations and vendor exhibits, ITherm 2018 will have panel discussions, keynote lectures by prominent speakers, invited Tech Talks, and professional short courses. All papers will be peer reviewed and published in the ITherm proceedings. Student first authors will have the opportunity to apply for ITherm travel grants in order to make an oral presentation and participate in a Student Poster and Networking Session.
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Use of the Monte Carlo Method in Packaging Thermal Calculations

Reprinted from the December, 2014, Issue

Bruce Guenin
Assoc. Technical Editor

INTRODUCTION

The state of the art in performing thermal calculations in our industry is very advanced. However, how applicable the results of a calculation are to the real-world performance of a packaging or an active cooling component depends on the quality of the data characterizing these various components. In the real world of manufacturing, such characterization parameters can never be a single value, but are always rep-resented by a statistical distribution.

Thermal calculations performed by engineers in our industry most often deal with nominal values of performance parameters that represent the design objective for a particular component rather than the result of a rigorous statistical analysis of detailed test results of its actual thermal performance. This sort of model is referred to here as a "deterministic model" [1].

This practice does not adequately address the risk that a component or system will not meet its thermal performance objectives. This article discusses the use of the Monte Carlo Method in that regard. It provides a surprisingly efficient process for adapting a deterministic model to account for the statistical variability of manufacturing and operational parameters that have a significant effect on the operating temperature of critical electronic devices.

THERMAL MODEL

The system to be analyzed here and the thermal model characterizing it have been discussed in previous installments of this column [2, 3, 4]. It is depicted in *Figure 1*. It consists of a flip-chip package with a copper lid to which a heat sink is attached. The package design is representative of those used for high pin count, high power ICs, with dissipated power levels in excess of 50W. The dominant heat flow path is from the active surface of the die (facing the substrate), up through the silicon, through the TIM1 layer (TIM = thermal interface material), the copper lid, the TIM2 layer, and into the heat sink whence it transferred into a flow-ing air stream. The heat flow path through the substrate and into the PCB (printed circuit board) represents only a small fraction of the total dissipated heat and is neglected here.

The TIM1 and TIM2 layers account for most of the variability in the thermal resistance path between the chip and the air. This is due to their much lower thermal conductivity then the other components and the variability in their thickness.

Reference 2 presents the design assumptions and calculated thermal results for 36 different configurations, representing different heat sink width, base thickness, thermal conductivity, and effective heat transfer coefficient (representing the cooling effect of the heat sink fins at dif-ferent assumed values of air velocity). Configuration #31 is assumed here. [*Reference 4* deals only with Configuration #31. It provides the details of this configuration in a more readable form than *Reference 2*].

TABLE
LIST OF PARAMETERS VARIED

PARAMETER	MEAN VALUE	STD DEVIATION		
		%	Value	Units
TIM1 THICKNESS	0.10	20%	0.02	mm
TIM2 THICKNESS	0.05	10%	0.005	mm
POWER, HI	80	10%	8.0	W
POWER, MED	70	10%	7.0	W
POWER, LO	60	10%	6.0	W
AMBIENT TEMP	22		3.0	°C

Table 1

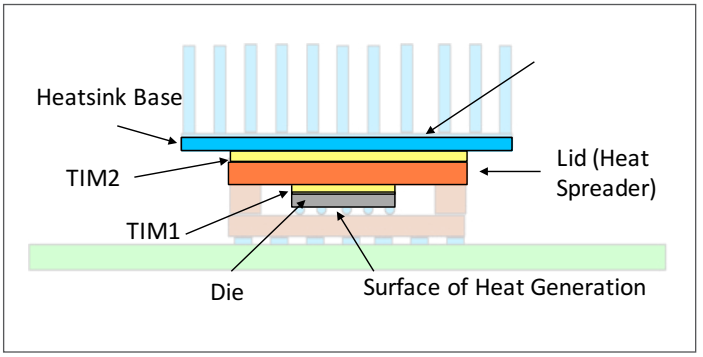


FIGURE 1. Diagram of high-power package attached to a heatsink. Components in bold color are explicitly represented in the model. Those in a faint color are part of the physical assembly, but are not represented in the model.

For configuration #31, the calculated value of Θ_{JA} = 0.87 ˚C/W. The assumed thickness and calculated thermal resistance for the two TIMs are as follows: TIM1: 0.1 mm, 0.296 ˚C/W; TIM2: 0.05 mm, 0.163 ˚C/W. Their combined thermal resistance is 0.46 ˚C/W and represents roughly 50% of the total thermal resistance. Variations in their thickness will have a significant effect on the ultimate value of Θ_{JA}. The relationships between the thermal resistance of the TIM1 and TIM2 layers and their thickness are provided by the following two equations:

$$\Theta_{TIM1}=\frac{t_{TIM1}}{k_{TIM1}*DieArea}=2.96*t_{TIM1}\,^{\circ}C/W \quad (1)$$

$$\Theta_{TIM2}=\frac{t_{TIM2}}{k_{TIM2}*HTA}=3.27*t_{TIM2}\,^{\circ}C/W \quad (2)$$

where the TIM thickness values, t_{TIM1} and t_{TIM2}, are in mm units. HTA is defined as the Heat Transfer Area through TIM2 = 17.5 mm *17.5 mm = 306 mm^2 [3,4]. The die area = 13 mm * 13 mm = 269 mm^2. The TIM1 and TIM2 materials are silver-filled epoxy and a metal-filled grease, respectively. The thermal conductivity values, k_{TIM1} and k_{TIM2} are equal to 2 W/mK and 1 W/mK, respectively.

The following expression provides the calculated value of Θ_{JA} as a function of the newly calculated values of Θ_{TIM1} and Θ_{TIM2}:

$$\Theta_{JA,NEW}=0.87+(\Theta_{TIM1,NEW}-0.296)+(\Theta_{TIM2,NEW}-0.163)\,^{\circ}C/W \quad (3)$$

Note that when $\Theta_{TIM1,\,NEW}$ and $\Theta_{TIM2,\,NEW}$ are equal to their original values, $\Theta_{JA,\,NEW}$ is equal to its original value also, as would be expected.

The final junction temperature of the die is calculated using $\Theta_{JA,\,NEW}$ the dissipated power, and the ambient air temperature using:

$$T_J = P*\Theta_{JA,NEW}+T_A \quad (4)$$

STATISTICAL ANALYSIS OF VARIATIONS IN A SINGLE PA-RAMETER

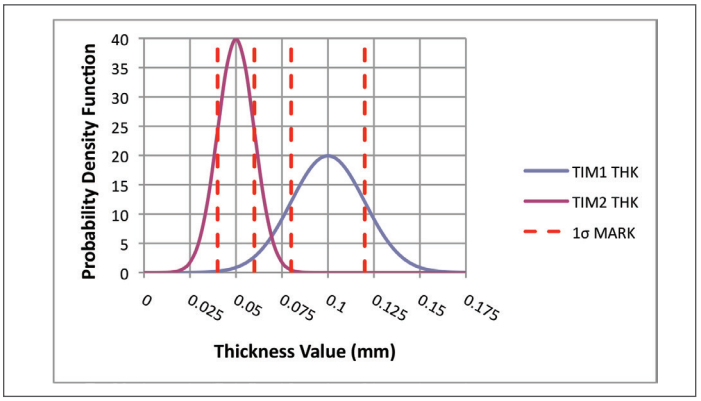
The next step in this process is to quantify the variability in the thickness of the TIM1 and TIM2 layers. This would normally begin with the measurement of these parameters on a population of randomly selected parts from the manufacturing line.

The results would be plotted in the form of a histogram and an appropriate function fitted to the data. In most cases, a normal (or Bell Curve) distribution is found to be effective in representing the variations of data of this sort [5].

Figure 2a displays a graph containing two normal distributions, each representing the statistical variation of the thickness of one the two TIMs. The mean values and standard deviations of these curves are provided in the Table. The curves are produced in a spreadsheet using the function:

NORMDIST(*Thickness, Mean Value, Std. Deviation*, FALSE) (5)

In order to embed this function in a spreadsheet to generate the curves, a column of ascending thickness values needs be created. A second column is populated with the NORMDIST function, with the Thickness argument in each occurrence of the function linked to the appropriate thickness value in the neighboring column.



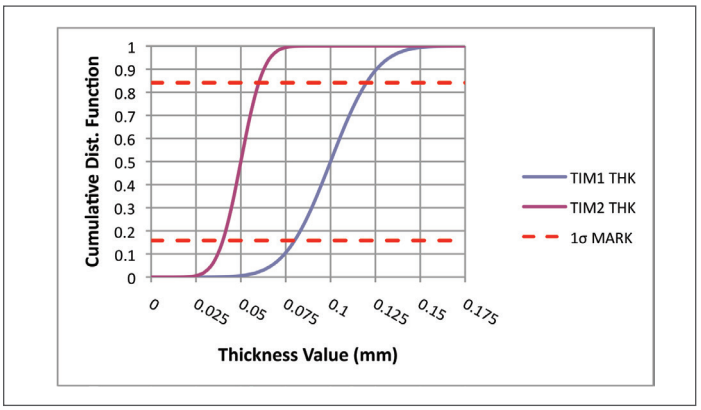


FIGURE 2a and 2b. Statistical distributions of thickness values for TIM1 and TIM2 per the values of mean value and standard deviation listed in the Table. Dotted lines bracket a single standard deviation in the graphs.

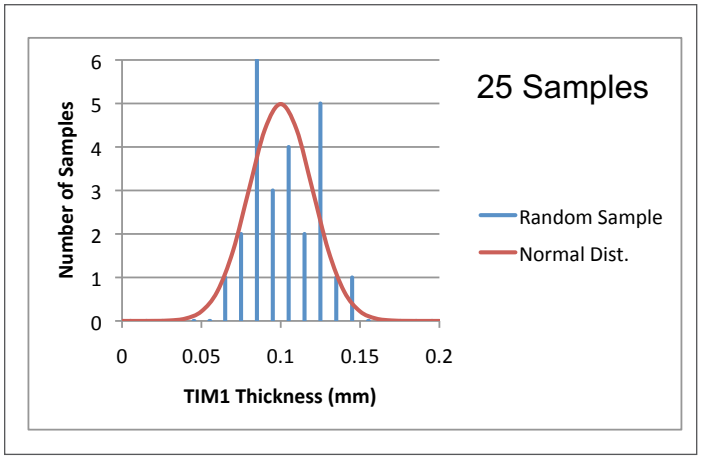
These curves are referred to as Probability Density Functions. Note that the distribution of the TIM2 thickness data is more peaked than for TIM1 due to having a smaller standard deviation (0.005 mm vs 0.02 mm). The dashed red lines mark the width of a single standard deviation on each graph. The graph in *Figure 2b* is displays the Cumulative Distribution Functions, based on the Probability Density Functions in 2a. Generally, a Cumulative Distribution Function is produced by a numerical integration of its respective Probability Density Function from minus infinity to plus infinity.

It provides a convenient means for determining the percentage of the total sample population having thick-ness values in an arbitrary range. The dashed red lines in the figure bracket a fraction of the total sample population equal to a single standard deviation or 68.3% of the total. These Cumulative Distribution Functions were generated in a spreadsheet using the function:

NORMDIST(*Thickness, Mean Value, Std. Deviation*, TRUE) (6)

APPLICATION OF MONTE CARLO METHOD

"Monte Carlo simulation is a type of simulation that relies on repeated random sampling and statistical analysis to compute the results. This method of simulation is very closely related to random experiments, experiments for which the specific result is not known in advance" [1].



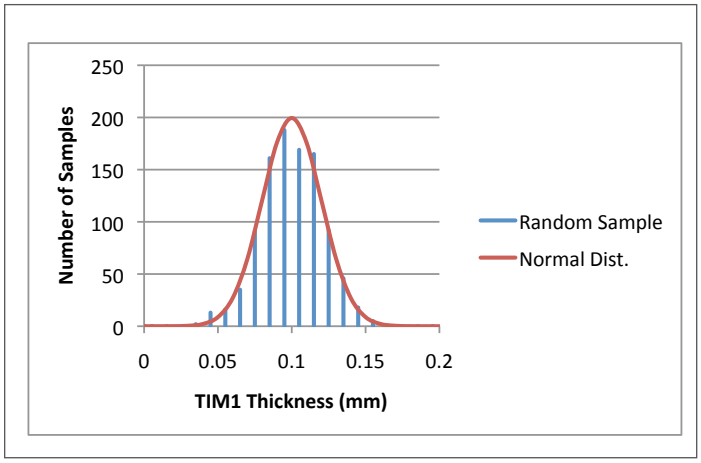


FIGURE 3a and 3b. Histograms generated using random sampled outputs from the Inverse Cumulative Distribution Function for TIM1: a) 25 samples; b) 1000 samples.

The method requires the Inverse Cumulative Distribution Function to generate a randomly sampled population of thickness values consistent with the statistics in the original Probability Den-

sity Function. This inverse function has the following form in the spreadsheet:

NORMINV(*Thickness, Mean Value, Std. Deviation*) (7)

In a spreadsheet, this is accomplished by linking the Thickness argument in the spreadsheet NORMINV function to a cell containing the random number function divided by an appropriate constant; such as:

RANDBETWEEN(1,9999)/10000 (8)

Note that this function randomly generates numbers between and including the limits: 1 and 9999. After the division by 10,000, these limits become: 0.0001 and 0.9999.

Figures 3a and *3b* are the output of such a process. In *3a*, only 25 random samples were generated. The resultant histogram deviates significantly from the Probability Density Function representing the original data. However, *Figure 3b*, the histogram generated using 1000 random samples tracks the original distribution well.

LINKING OF RANDOM SAMPLING OF TIM1 AND TIM2 THICK-NESS TO THERMAL MODEL

The histogram in *Figure 3b* can be used to generate an equivalent distribution of Θ_{TIM1} values by inputting each randomly sampled value of TIM1 thickness into *Eqn. 1*, and similarly for $\Theta_{TIM2.}$ The resultant thermal resistance distributions are plotted in the graph in *Figure 4*.

Randomly selected pairs of sampled values of Θ_{TIM1} and Θ_{TIM2}. from these distributions are input into *Eqn. 3* to generate the associated distribution of Θ_{JA} values, which is plotted on the right side of *Figure 4*.

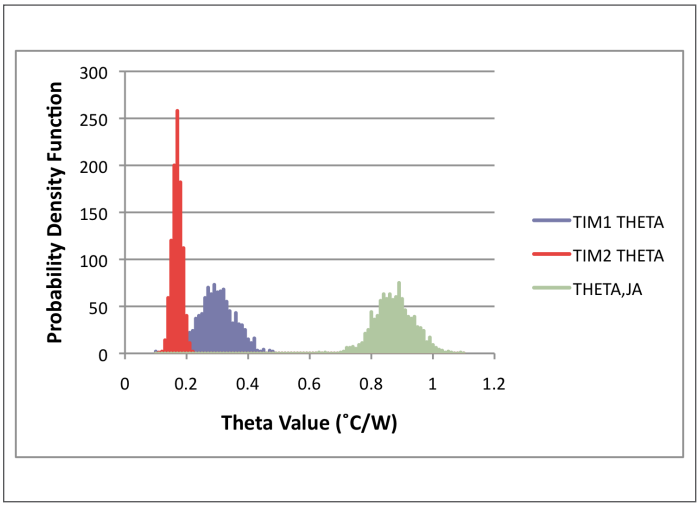


FIGURE 4. Probability Density Function for calculations of:
1) Θ_{TIM1} and Θ_{TIM2}, based on TIM1 and TIM2 thickness distributions and Eqns. 1 and 2.
2) Θ_{JA}, based on Θ_{TIM1} and Θ_{TIM2} distributions and Eqn. 3.

CALCULATION OF JUNCTION TEMPERATURE DISTRIBUTION UNDER VARIOUS POWER ASSUMPTIONS

This final stage of the calculation is intended to predict the highest allowed power consistent with having a high probability that T_J will not exceed a specified value, which is normally chosen for reliability reasons. In this case, the T_J limit is set at a typical value of 90C.

The Table displays the mean values and standard deviations for three different power distributions and also for ambient temperature. In order to implement the generation of different junction temperature distributions based on these different inputs the same procedure as before is implemented:

1. Create the Probability Density Function using the appropriate spreadsheet function.

2. Use the random number function as an input to the Inverse Cumulative Distribution Function, using the same mean value and standard deviation, to generate a random sampling of power levels and ambient temperatures.

3. Input these values of power levels and ambient temperatures along with the previously generated distribution of Θ_{JA} values into *Eqn. 4*.

The histograms representing the output of *Eqn. 4* in response to the input of the random samplings of Θ_{JA}, power, and ambient temperature values are shown in *Figure 5a*. *Figure 5b* depicts the Probability Density Function created by simply plotting the values of the histogram in an x-y plot.

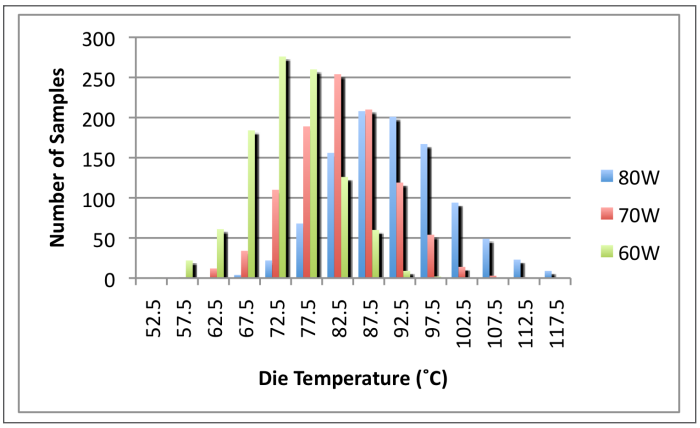


FIGURE 5a. Histogram of calculated distribution of die temperature based on Θ_{JA} distribution and normal distributions of ambient temperature and power and inputting these values into Eqn. 4.

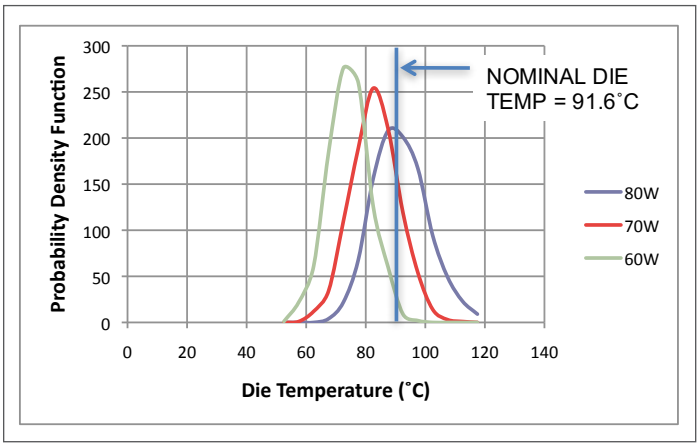


FIGURE 5b. x-y plot based on data in Fig. 5a.

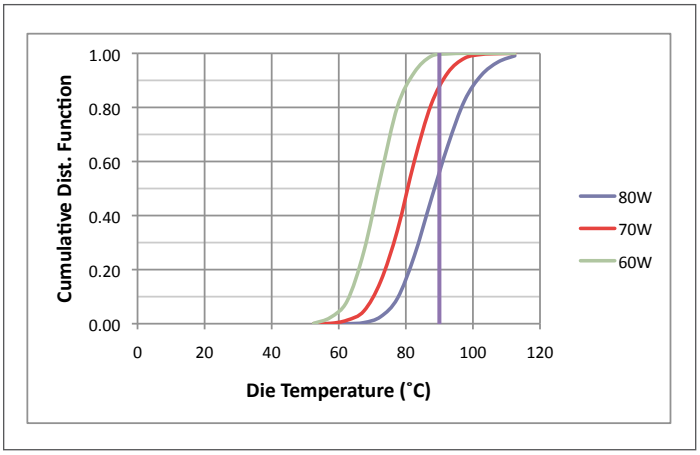


FIGURE 5c. Cumulative Distribution Function obtained by numeri-cal integration of curves in Fig. 5b.

The associated Cumulative Distribution Function is plotted in *Figure 5c* and was created by performing a simple numerical integration in the spreadsheet.

The value at any particular value of junction temperature was generated by adding up all of the values in the distribution to the left of the location to the value at that location. This analysis shows the following percentage of systems that would have a T_J in excess of 90C: 80W, 44.2%; 70W, 13.1%; 60W, 0.6%.

It is useful to compare these findings from applying the Monte Carlo Method to the thermal problem at hand compared with a calculation based on the mean values of all the parameters involved. Plugging the mean values of the param-eters into *Eqns. 1 – 4* yields a predicted junction temperature of 91.6C at 80W. One might then decide that this 80W value need only be reduced by a few watts to get the maximum value of T_J within acceptable limits. However, based on the Monte Carlo analysis performed here, one sees that making that decision would lead to over 40% of the devices having junction temperatures exceeding the design limit.

CONCLUSIONS

This analysis is intended to demonstrate the mechanics of the Monte Carlo Method in determining allowable power levels for a relatively simple electronics cooling application. However, the method is well capable of scaling to a much higher degree of complexity to deal with situations involving many more design parameters than the situation explored here. Furthermore, the method can readily be adapted to deal with Probability Density Functions other than normal distributions. All that is necessary is that a suitable function or numerical method be constructed to replicate the experimentally derived distribution. This function would then be used to calculate the Inverse Cumulative Distribution Function that is needed to generate the random sampling of simulated outputs from the thermal model.

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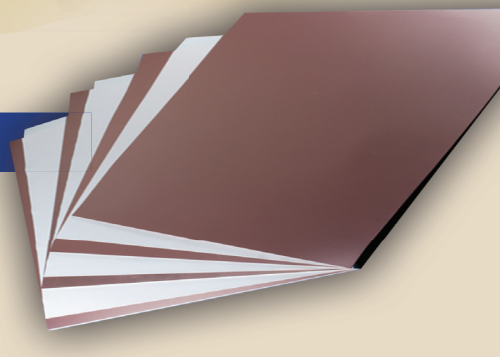

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The Junction-to-Case Thermal Resistance: A One-Dimensional Underachiever in a Three-dimensional, Conjugate Heat Transfer World

Bruce Guenin
Assoc. Technical Editor

INTRODUCTION

As integrated circuits were becoming more widespread in the 1980's, most of the developmental problems had to do the with electrical operation of the devices and not so much on cooling them, due to low power levels. It was the electrical engineers who did the functional testing, an activity that ultimately expanded to include thermal testing. Even the thermal tests were largely an electrical exercise since temperatures were measured on silicon using diodes and elsewhere using thermocouples. The term "thermal resistance" became popular during this period when an electrical-engineer-centric culture dominated package design and development. This culture also gets credit for describing the flow state of the air when thermally testing a package in a closed box as "still air" rather than as "buoyancy-driven convection" or "natural convection", as a thermal engineer would more accurately describe it.

Specifically, the package thermal metric, "junction-to-case thermal resistance" or Θ_{JC} (Theta,jc) was defined and test methods prescribed at that time in Military and SEMI specifications [1]. These methods offered a choice of using either a fluid bath or a heat sink environment. They assumed that the measured Θ_{JC} results are independent of the particular environmental heat flow conditions and that the value of Θ_{JC} is an intrinsic property of the package, similar to the very convenient situation involving electrical resistors [1]. These beginnings in the life of the Θ_{JC} metric apparently set the stage for confusion that continues to this day.

The rigor in thermal standards improved considerably after the founding of the JEDEC JC-15 Thermal Standards Committee in 1990. In fact, the committee charter includes the following requirements for their standards:

- These standards shall be meaningful, consistent, and shall be proven to be scientifically sound
- The standards will provide a common means of comparison of thermal phenomena for users of microelectronic packaging

During the 1990s, this committee made a significant contribution to the thermal testing of microelectronic packages by creating precise specifications for thermal test chips, test boards for mounting of a large number package types, and a variety of test environments. These environments include natural and forced convection and the junction-to-board thermal resistance conduction test environment and performing the initial work in the development of a robust junction-to-case standard [2, 3]. It should be noted that all the test boards for a particular package style are available in low- and high-conductivity versions, differing in the amount of copper in the board to control the amount of heat spreading by the board under test.

These test environments were inherently simplified, as compared with the extreme diversity of the actual application environments. Examples include the specification of a single, uniform heat source on the test die and laminar air flow in a wind tunnel. However, these simplifications made it easier for labs to implement the standards precisely and reduced the number of possible test conditions for a particular package design. This was consistent with the mission to provide a consistent basis for comparison of the thermal behavior of competing package designs.

Of course, then as now, thermal engineers are called upon not only to choose the package with the best thermal performance out of the available options, but also to predict chip temperatures in the end-use environment. In those earlier days, when thermal modeling was much less advanced, thermal engineers had to make best use of the information they had at hand. Θ_{JC} was a convenient thermal parameter when it was necessary to estimate the temperature of a device mounted to a heat sink. Nowadays, with the availability of more powerful simulation tools and the development of more complex thermal resistance networks for representing realistic heat flows within a package, we can do much better than that [4]. Even now, there are instances when a quick, spreadsheet type network resistor model can be very useful and a Θ_{JC} value a necessary part of the calculation.

It is possible to use the Θ_{JC} metric intelligently, as long as the engineer understands its limitations. The next two sections are devoted to increasing the reader's awareness of certain subtleties in measuring Θ_{JC} and in its use in predicting chip temperatures in a package with a heat sink mounted to it. They are based on an earlier

installment by this author in the column, Calculation Corner. [5]

TWO CASE STUDIES

1. Simulation of Θ_{JC} Test Environment

The junction-to-case thermal resistance, Θ_{JC}, is calculated using the following equation, which has the same form as Ohms Law for electrical resistances:

$$\Theta_{JC} = \frac{(T_J - T_c)}{P_{JC}} \quad (1)$$

where T_J is the junction temperature (on a JEDEC-standard test chip, it is located at the top center of the chip), T_C is the case temperature, normally measured at the top, center of the test package, and P_{JC} is the dissipated power flowing from the junction to the case and then into the heat sink provided by the test apparatus. Note that P_{JC} is normally less than the total dissipated power, P_T, because usually some of the heat is lost to the environment. There are ways of determining the heat lost from the test package so that P_{JC} can be accurately calculated [5].

The analysis below, explores the accuracy of a Finite Element Analysis (FEA) conduction model to predict the Θ_{JC} test result for two configurations of a popular PBGA (Plastic Ball Grid Array) package.

Figure 1 displays various graphics outputs from the FEA model, showing both the external and internal construction of the low-conductivity and the high-conductivity package mounted to a high-conductivity JEDEC-standard thermal test board.

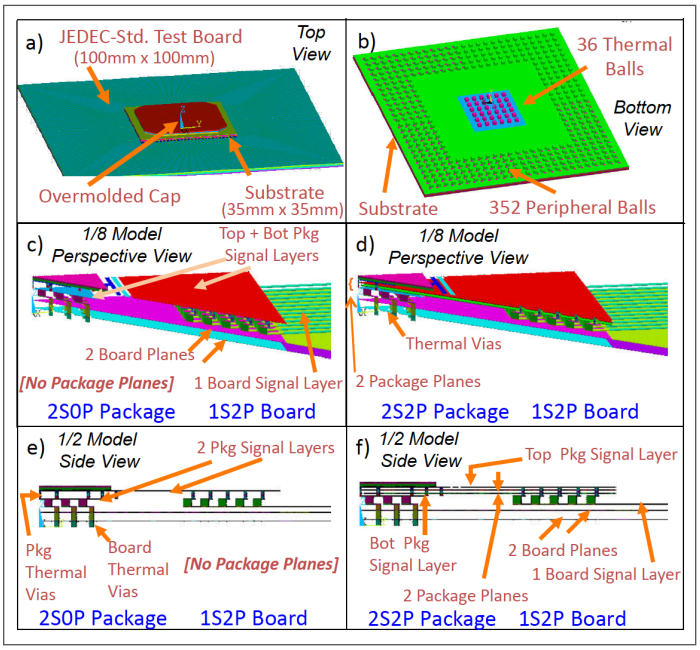

Figure 1: Graphics output from FEA model showing both the external and internal construction of the package and board designs involving in this study.

Figure 2 shows temperature contour maps output by the FEA simulation involving the test package on a high-conductivity JEDEC-standard test board in the JEDEC Θ_{JC} test environment. The stated values of Θ_{JC} were calculated from these results using *equation (1)*. In this manner, Θ_{JC} was determined for the 2S0P package to be 6.2 C/W and that for the 2S2P package to be 4.8 C/W. These values compare favorably with the experimentally measured values, 6.1 C/W and 5.5 C/W, respectively. This example illustrates an important use of Θ_{JC} test results, namely, verifying the accuracy of the representation of the internal structure of the package in the model.

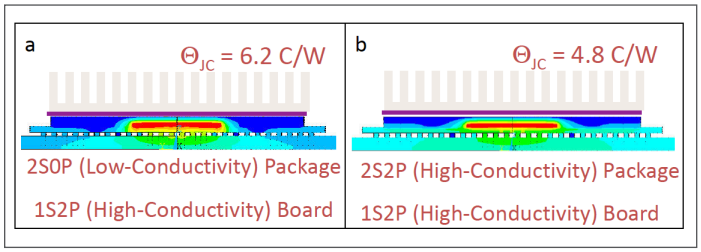

Figure 2: Results of FEA thermal simulation involving low- and high- conductivity packages on low- and high- conductivity JEDEC-standard test board in the JEDEC Θ_{JC} test environment.

2. Thermal interactions between air, test board, and heat sink in wind tunnel test

This example deals with the same package design as in the previous section, but only with the 2S2P laminate configuration and with the 1S2P test board.

The analysis begins with a consideration of how to predict the junction temperature in a package with a heat sink attached to it, based on 1) thermal measurements on the package/board assembly in a wind tunnel and 2) thermal measurements made on the heat sink by its manufacturer.

The approach explored here will involve the generation of thermal resistance values for the package and board which were generated using a method described in a previous column. Specifically, the inputs to the calculation consisted of all four of the measured temperatures for the package without a heat sink (shown in *Figure 3a*), the total dissipated power, and the calculated heat transfer coefficient [6]. A value for Θ_{SA} was taken from the manufacturer's data sheet for the velocity of interest, 0.5 m/s.

Such a simple resistor-network conduction model normally accounts for heat loss to the ambient by applying a heat transfer coefficient to external surfaces assuming a global value of ambient temperature. The heat transfer coefficient can be calculated to account for buoyancy-driven convection, forced convection, and radiation heat transfer. However, it cannot account for conjugate heat transfer, in which the air flow and the subsequent transport of heat from one region to another in the model are explicitly calculated.

Figure 3a depicts the conduction of heat by the package and board from the chip to the ambient air. *Figure 3b* adds the heat sink to the top of the package. The extended area of the heat sink

promotes more efficient heat transfer to the flowing air than is possible with the bare package top. However, the limitations of this simple conduction model assume that the temperature of the ambient air is not changed by the flow of heat from the solid surfaces into it. The pattern of red arrows (representing heat flow) are intended to represent this situation.

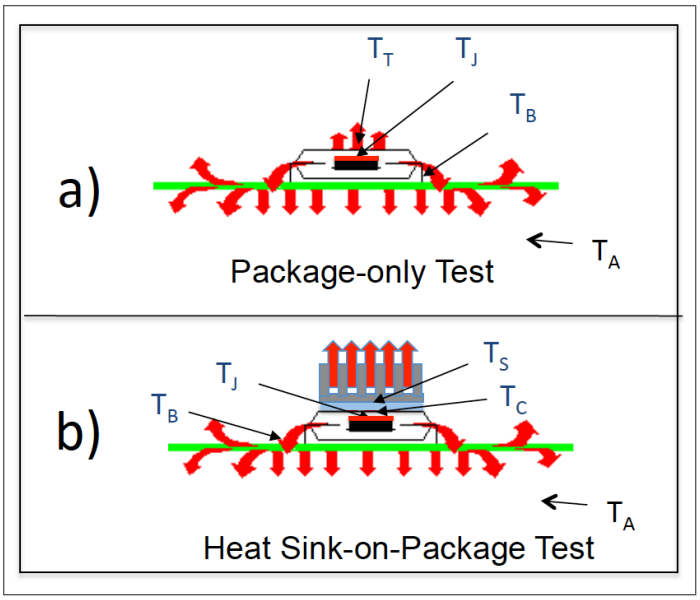

Figure 3: Diagram showing heat flow out of an arbitrary package in a wind tunnel environment as represented in a conduction model in which the loss of heat to the ambient air was accounted for using a heat transfer coefficient.

Figure 4 provides a schematic of a thermal resistor network that represents the two paths followed by the heat flow from the chip in the package. The first path is directed upward to the top of the package. The first resistor along this path is Θ_{JC}. If no heat sink were present, the heat would then flow directly into the ambient air. The efficiency of this heat transfer process is represented by the case-to-air thermal resistance, Θ_{CA}. If there is a heat sink present, then the heat flow through the heat sink into the air is represented by the sink-to-air thermal resistance, Θ_{SA}. The downward flow of heat from the chip is represented by the two thermal resistances: junction-to-board, Θ_{JB}, and the board-to-air, Θ_{BA}.

The predictions of the thermal network model for Θ_{JA} for the package with the heat sink attached were compared to measured values of Θ_{JA} in a wind tunnel environment.

Table 1 lists values for all of the calculated thermal resistances. The predicted value of Θ_{JA} for the package without a heat sink present agreed very well with the measured value of 16.6 ˚C/W. This is what would have been expected and simply confirms that the calculation based on solving the thermal resistor network was working properly.

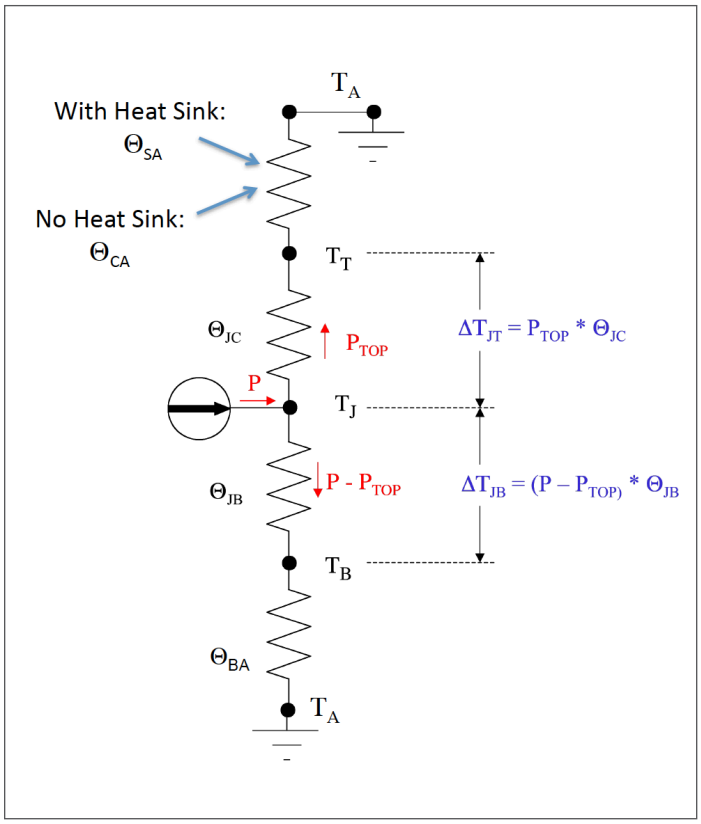

Figure 4: Thermal resistor network representing the heat flow situations in Figure 3. Note that the top resistor (terminating in the ambient air) is assigned the value of Θ_{CA} when no heat sink is present and Θ_{SA} when one is.

The same calculation was repeated with the exception that Θ_{SA} was substituted for Θ_{CA}. All the other resistor values were kept equal to those used in the calculation without a heat sink present.

Table 1
Final Calculated Thermal Resistance Values and % of Total Heat Flowing Out Top and Bottom Paths
Package Laminate -- 2S2P; JEDEC High-Conductivity Board Design -- 1S2P
Aluminum Heat Sink -- 28mm x 28mm base, 8x8 Pin Grid Array -- Variable Height

Air Velocity	Power	Heat Sink, Height	UPWARD PATH					DOWNWARD PATH				ENTIRE CIRCUIT		
			RESISTOR VALUES			ENTIRE PATH		RESISTOR VALUES		ENTIRE PATH		RESISTOR VALUES		
			Θ_{CA}	Θ_{SA}	Θ_{JC}	$\Theta_{Up\ Path}$	% P_{Up}	Θ_{JB}	Θ_{BA}	$\Theta_{Down\ Path}$	% P_{Down}	Θ_{JA} CALC	Θ_{JA} TEST	$\Delta\Theta_{JA}$
(m/s)	(W)	(mm)	(˚C/W)	(˚C/W)	(˚C/W)	(˚C/W)	(%)	(˚C/W)	(˚C/W)	(˚C/W)	(%)	(˚C/W)	(˚C/W)	(%)
0.5	3	*N/A*	446	*N/A*	5.5	451	4%	11.1	6.1	17.2	96%	16.6	16.6	0.04%
		6	*N/A*	12.4	5.5	17.9	33%	11.1	6.1	17.2	67%	8.8	11.8	26%
		15	*N/A*	5.5	5.5	11.0	38%	11.1	6.1	17.2	62%	6.7	9.9	32%

The solution of the revised thermal network yielded Θ_{JA} values that were much smaller than the measured ones. The difference was 26% for the 6mm high heat sink and 32% for the 15mm high heat sink. This indicates that the real package was running considerably hotter than that predicted by the calculation.

Why did the calculation predict much cooler chip temperatures with the heat sinks present than were measured? An explanation can be found by examining *Figure 5*.

Figure 5 provides diagrams representing conjugate heat exchange with the flowing air for three test conditions involving either a) the package attached to a board or b) the heat sink with an attached heater, or c) the heat sink mounted to the package/board assembly. It indicates that in case (c), both the package/board and the heat sink are not cooled as efficiently by the airflow as when they were tested separately. This is due to a combination of preheating of the air the flowing into heat sink and to the reduction of the air velocity in the downstream half of the board.

The bottom line is that neither the board nor the heat sink are cooled as effectively when they are attached to each other compared to when they were tested separately.

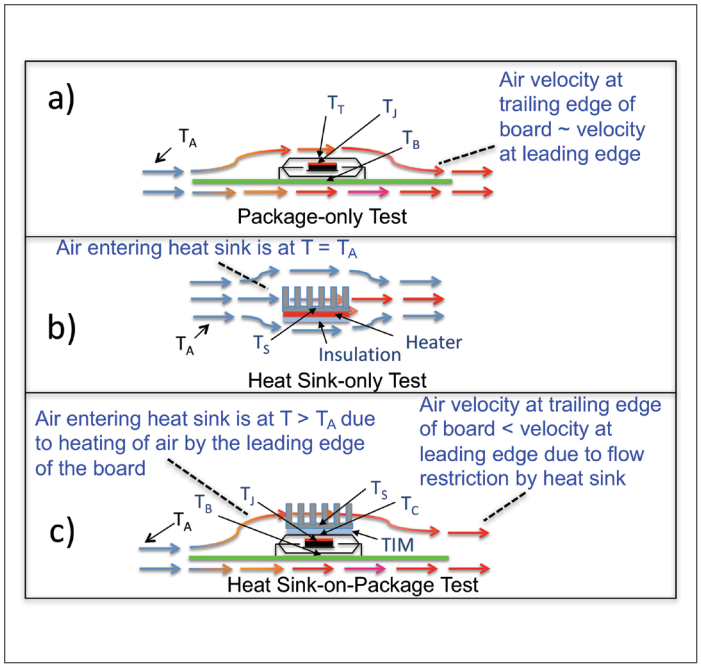

Figure 5: Diagrams representing conjugate heat exchange with the flowing air for 3 test configurations involving a package/board assembly and a heat sink.

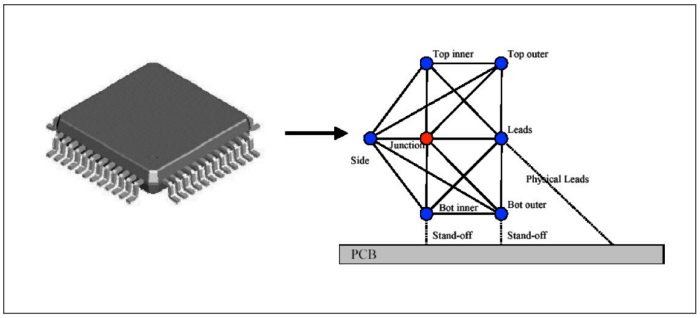

Figure 6: Drawing of a plastic leaded quad package accompanied by its thermal representation in a resistor network Compact Thermal Model generated using the DELPHI method [4]. Here the network is shown with a thermal connection to a solid entity, representing a PCB, in a CFD model. Similarly, it could be connected to a solid representing a heat sink at the top of the network.

RECOMMENDATIONS

The previous discussion made it clear that even a very simple system, such as a package attached to a board and a heat sink in a wind tunnel, cannot be accurately modeled unless the heat exchange between the solid surfaces and the flowing air is treated in a way that represents the complex physics of the heat transfer process.

However, even if the solution method accounted for this, say by using a modern computational fluid dynamics (CFD) program, there would still be problems with using thermal resistor elements that can only account for 1-dimensional heat flow. Fortunately, methods have been developed to create resistor networks that can simulate heat flows within a package representing thermal gradients that vary in three dimensions.

The JEDEC JC-15 committee has issued standards that apply what is known as the Delphi Compact Thermal Model (CTM) methodology to generate these resistor networks and integrate them into a model containing other components, such as circuit boards and heat sinks [4]. One such network is depicted in *Figure 5*.

The leading commercial CFD software tools serving the electronics cooling market have the capability for applying the CTM methodology. It is hoped that this article may help to raise the awareness in the industry of the benefit of applying CTM methods more widely than they are now.

The Θ_{JC} test method still serves an important function by enabling the comparison the thermal performance of competing packaging designs related to how efficiently they transport heat to an external heat sink. Also, the correlation of a detailed simulation of a package in the Θ_{JC} environment with the test result can serve to improve the accuracy of the thermal representation of the package internal structure in the model.

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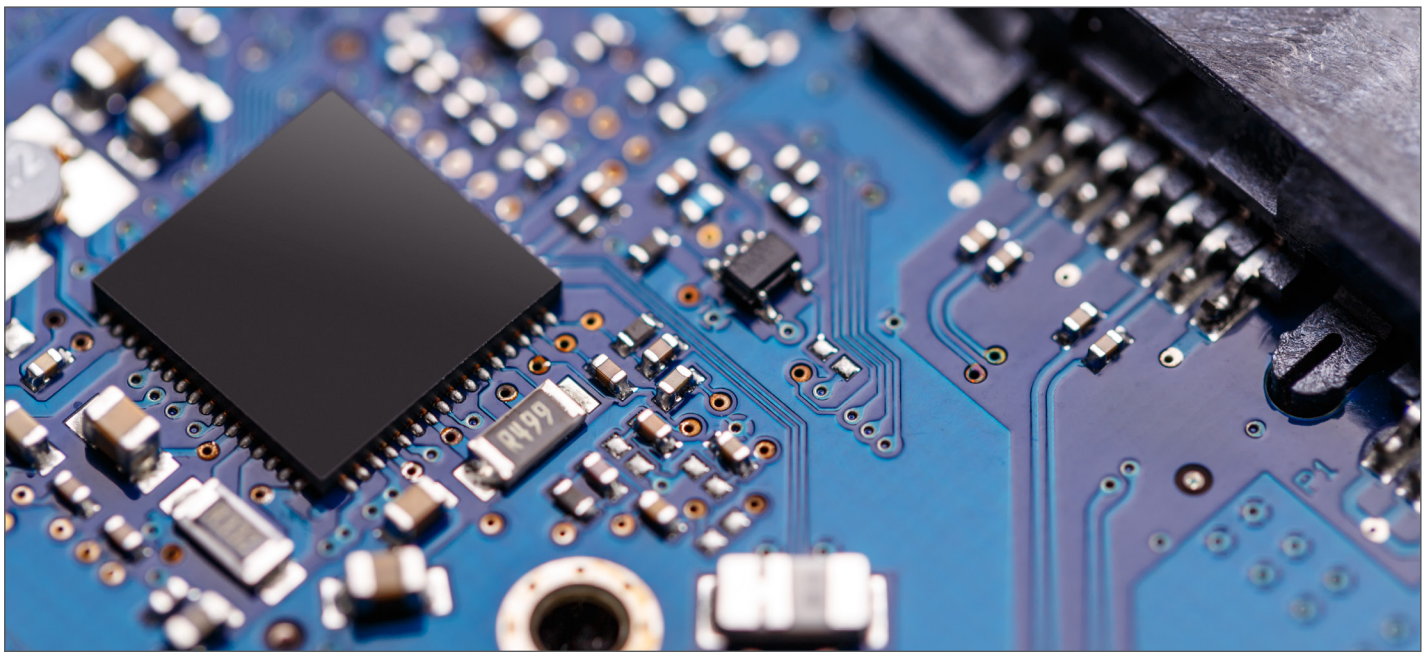

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THERMAL INNOVATIONS THAT MAKE THE WORLD'S TECHNOLOGY COOL

Developing a Theta$_{jc}$ Standard Under Steady-State Testing Conditions

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Eduardo de los Heros
Qualcomm Datacenter Technologies, Inc

ABSTRACT

Testing standards provide a common framework for collecting and reporting data. Without a clearly defined testing standard, it is impossible to compare experimental data measured by different labs since differing test conditions may mask the very effect being tested. For this reason, a Theta$_{jc}$ standard is needed to specify testing conditions that allow for an equitable comparison of data, such as to determine which assembly process or package style has a lower thermal resistance. This study presents a summary of test data collected for three different thermal test vehicles having Theta$_{jc}$ values of approximately 7°C/W, 2.5°C/W, 1.8°C/W and 0.07°C/W. Recommendations are provided on two different methods for measuring the case temperature depending on the Theta$_{jc}$ value in question. For Theta$_{jc}$ values less than a critical value, embedded case thermocouples should be attached to the case. Otherwise the thermocouple may be flush mounted to the surface of the heat sink.

INTRODUCTION

There are strong opinions on the relative merits for performing steady-state Theta$_{jc}$ tests. Lasance and Lacase [1] raised concerns on the time required to perform steady-state measurements. Also, they indicated steady-state tests are difficult to perform if high accuracy measurements are required. Others have indicated a reluctance to adopt a new test method since there is an historical precedent for continuing to use existing methods. There are many challenges that must be addressed including; the effects of power map, differences in heat sink design, differences in thermal interface material between case and heat sink (commonly referred to as TIM II), differences in sensing junction and case temperature and quantifying the dissipative power. Over the past 15 years, the JEDEC thermal standards committee, JC15, has worked on establishing a steady-state Theta$_{jc}$ standard but has not made significant progress due to many of these challenges.

Although progress on the steady-state Theta$_{jc}$ standard has languished over the years, the transient standard JESD 51-14 [2] was released and now is available. This standard was widely accepted for smaller packages that have a single heat transfer path. However, for larger packages, such as a flip chip ball grid array (FCBGA) package, two heat flow directions are present (between the active side of the die and the case and between the die and substrate). Presently, transient testing cannot experimentally quantify the power distribution between the top of the package and through the board. Therefore, the transient method cannot be applied to large packages with two directions of heat flow. Steady-state testing also provides a more realistic testing condition because it allows the test package to reach a temperature profile similar to the functional package operating at its desired power level. As a result, factors controlling Theta$_{jc}$, such as the temperature-dependent material properties and package warpage, will more closely represent those found in a functional package.

Table 1. Applicability set of conditions for the Theta$_{jc}$ tests

#	Restriction	Reason for Restriction
1	Thermal die only	Functional die add uncertainty due to non-uniform power maps, difficulty in determining power dissipation and difficulty in measuring the junction temperature in the center of the die.
2	Low resistance heat sink or cold plate.	For heat sinks with low conductivity base materials, Theta$_{jc}$ is affected by the thermal conductivity of the base material. It is recommended that a high conductivity material be used, e.g. k ≥ 380W/m-K.
3	Case temperature measured with a thermocouple or embedded thermocouple in the heat sink or cold plate.	A thermocouple is small, simple to use and widely available. Other temperature sensing methods are possible, see [4], but are not necessarily recommended.
4	Produce a uniform heat flux across die surface.	Provides a common boundary condition and meets JEDEC standard for a test die, [5].
5	Case temperature measured at center of package.	For a uniform heat flux condition, the hottest case temperature should be at the center of the case.

Various methods for measuring the case temperature are outlined in Galloway and Okpe [3], however; based on the experience of the authors, the thermocouple is a better choice for measuring case temperature. $Theta_{jc}$ measurement uncertainties attributed to instrumentation are discussed in De Los Heros *et al.* [4]. Rather than address all the expressed concerns, the proposed standard restricts the set of conditions to those most easily controlled and more commonly employed when making $Theta_{jc}$ measurements. *Table 1* summarizes the restricted set of conditions considered for the proposed $Theta_{jc}$ standard. It is understood that, in some cases, not all conditions will be satisfied. The tradeoff in making the standard less restrictive is that there may be greater variability in results when testing the same packages.

The factors that guided the development of the $Theta_{jc}$ standard include; ensuring that the method is based on sound scientific principles, the data produced from the testing are useful and reproducible and that the equipment needed for the testing is readily available and not overly expensive.

TESTING OVERVIEW

$Theta_{jc}$ is defined in *equation (1)* and includes the measurement of the junction temperature, T_j, case temperature, T_c, and power, P_c, leaving the case of the package.

$$Theta_{jc} = \frac{T_j - T_c}{P_c} \quad (1)$$

The power, P_c, required to evaluate *Equation (1)* will be lower than the supplied electrical power because it must not include the heat loss to the surroundings. An estimate of the heat loss should be provided using finite element analysis (FEA) or by other means. The heat loss, predicted using FEA, was 7% for a low-power package and 3% for two other high-power packages. An experimental method may be employed to approximate the heat loss by placing an insulating sheet of material (e.g. 2mm thick Teflon sheet) between the heat sink and the test vehicle. This allows a lower power setting to produce a similar junction temperature as measured during $Theta_{jc}$ tests. The amount of electrical power used to power the insulated package can be used as an approximation for the heat loss. Heat losses should be minimized by using proper insulating materials, see for example the insulating backing plate shown in *Figure 1*.

EXPERIMENTAL SYSTEM

The design and selection of the testing apparatus was made as simple as possible without taking away from the accuracy of the $Theta_{jc}$ test. A central processing unit (CPU) cooler was used as the cooling sink since it is widely available and is relatively inexpensive compared to a cold plate; however, it is more susceptible to ambient temperature variations. The CPU cooler has a case-to-ambient resistance of approximately 0.12C/W. It was fabricated using copper plate fins and a 7mm thick copper base. *Figure 1* shows the test system including the CPU cooler, test board, insulated backing plate and a weight used to apply clamping pressure between the package and the heat sink.

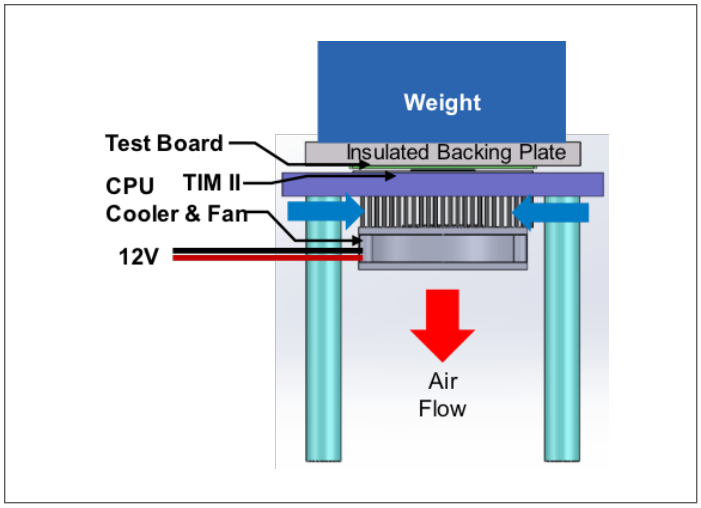
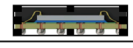
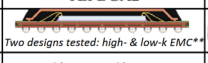
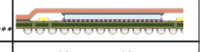
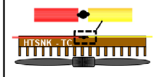
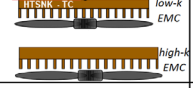
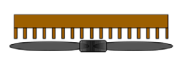


Figure 1. CPU test system.

Three different test boards were selected including a carrier array ball grid array (CABGA) package, thermally enhanced plastic ball grid array (TEPBGA2) package and a flip chip ball grid array (FCBGA) package. A summary of the package information is included in *Table 2*. Two different CPU coolers were used based on the value of $Theta_{jc}$. For high $Theta_{jc}$ values, a CPU cooler having an embedded thermocouple (TC) was used to measure the case temperature since the resistance of the thermal interface material between the case and CPU cooler (TIM II) was small in comparison to the value of $Theta_{jc}$. This led to a slightly lower temperature measurement at the base of the CPU cooler than the package case. This simplifies testing since only one TC must be installed in the heat sink when testing multiple parts. Because the CABGA package has a relatively high $Theta_{jc}$ value, the embedded thermocouple CPU cooler was used. Similarly, the TEPBGA2 packages 3, 4, and 5, which were manufactured with low conductivity mold compound, used the embedded heat sink thermocouple to measure $Theta_{jc}$.

TEPBGA2 packages 1, 2 and 6 were manufactured using a high conductivity mold compound resulting in a lower $Theta_{jc}$. The FCBGA package had an even lower $Theta_{jc}$ value. Both these package types required embedded case thermocouples to accurately measure $Theta_{jc}$ and did not use a thermocouple in the CPU cooler.

Table 2. Summary of package dimensions and test conditions

	CABGA	TEPBGA2	FCBGA
Package		 Two designs tested: high- & low-k EMC**	
Body size	12 mm x 12 mm	40 mm x 40 mm	40 mm x 40 mm
Die size	7.78 mm x 7.78 mm	10.16 mm x 10.16 mm	16 mm x 16 mm
Pressure*	68 KPa	56 KPa	51 KPa
CPU cooler			
Ave Theta jc	7.0°C/W	1.8°C/W *(high-k EMC)* and 2.5°C/W *(low-k EMC)*	0.07°C/W
Total pkgs tested	(6)	(6)	(6)

* Pressure based on exposed lid surface area in contact with CPU cooler.
** EMC = Epoxy Molding Compound

Fine (40 gauge) thermocouples, with polymer insulation in a duplex wire format, having outer dimensions of approximately 800 µm x 400 µm, were selected to measure the package case temperature and the CPU cooler temperature. The required cross-section area of the thermocouple may be reduced by removing the outer insulation and separating the positive from the negative leads so that the leads extend outward in a co-linear orientation. A diagram of the split thermocouple is shown in *Table 2* for the CABGA package. The single insulated thermocouple wire has a diameter of approximately 200 µm. A 250-µm wide x 350-µm deep groove was milled across the surface of the case and the heat sink surface. Type K thermocouples (chromel-alumel, i.e., nickel alloys) were selected since they are mechanically more robust then type T (copper-constantan) thermocouples. Type K TCs also have a lower thermal conductivity and will have a smaller effect on temperature measurements in regions of high thermal gradients. The thermocouple was inserted into the groove and pushed down to make contact with the bottom of the groove. Silver epoxy was placed above and around the TC and was planarized smooth with the surface of the case or heat sink. The TC bead made contact with the copper case or copper heat sink.

EXPERIMENTAL RESULTS

To confirm the repeatability of $Theta_{jc}$ measurements, a round-robin test was conducted by three different test engineers. Ideally, data measured by one engineer should agree with measurements made by another. To improve the likelihood of achieving this goal, common fixturing and testing methodology should be followed. A common set of boards were exchanged between test labs. The same set of calibration curves were used by all test engineers. The same data acquisition, TIM II and weights were also used in making measurements. The primary goal was to understand the $Theta_{jc}$ variability caused by the test engineer. Tests were performed by engineer 1 and engineer 2 at the same company and engineer 3 at a different company.

In each test, TIM II was deposited on the heat sink and thinned to 70 µm thickness using a flat spatula. The thickness was controlled by using two strips of Kapton tape placed on each side of heat sink to create a standoff that supported the TIM II application process. Weights applied to the insulation plate provided a downward force between the package and the heat sink. The weight was adjusted for each package based on the exposed area of each package. The CABGA has a small exposed area, therefore only a 0.5 kg mass was needed.

$Theta_{jc}$ data are shown in *Figure 4* as a function of the package number and engineer (1, 2 or 3). The standard deviation divided by the average of data taken by the three engineers for that package are shown in *Figure 5*. In general, the agreement between engineers for all packages is quite good. For most packages tested, the standard deviation between engineers is less than 2% of the average. $Theta_{jc}$ measurement for part C6 appears to be an outlier. The CABGA package showed greater deviation, especially for parts 1-4. This is not surprising because the CABGA with its small body size will be more susceptible to TIM II application variations compared to all other packages.

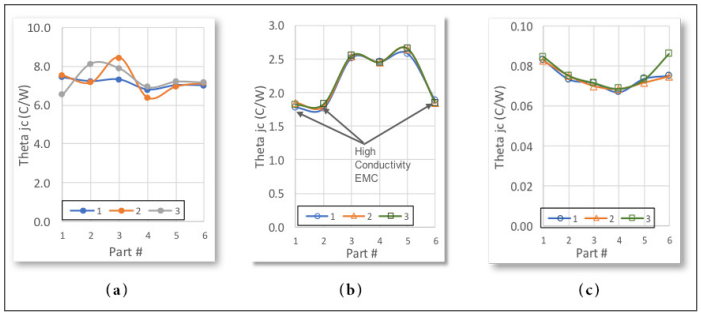


Figure 4. Comparison of experimental data (a) CABGA, (b) TEPBGA2, and (c) FCBGA.

Figure 5. Comparison of data as a function of part and test engineer.

An analysis was conducted to determine a critical $Theta_{jc}$ value for which the case temperature should be measured with an embedded thermocouple. This analysis was based on an assumed level of 5% uncertainty in $Theta_{jc}$ measurements due to the TIM II resistance contribution. A corrected case temperature measurement can be written in *Equation (2)*, using the portion of the power dissipated by the die.

$$T_c = T_{HTSNK} + P_c * Theta_{TIM\ II} \tag{2}$$

Substituting *Equation (2)* into *Equation (1)* yields:

$$Theta_{jc} + Theta_{TIM\ II} = \frac{T_j - T_{HTSNK}}{P_c} \tag{3}$$

When the heat sink temperature is used as the case temperature reference, the TIM II resistance must be less than the acceptable uncertainty. The critical $Theta_{jc}$ value may be calculated in *Equation (4)*.

$$Theta_{TIM\ II} \sim \frac{BLT}{K_{TIM\ II} * A_{Die}} < 0.05 * Theta_{jc} \tag{4}$$

where BLT is the bond line thickness and $K_{TIM\ II}$ is the thermal conductivity of TIM II. $Theta_{TIM\ II}$ may be approximated conservatively in *Equation (4)* by setting the heat transfer area equal to the die area. This is somewhat conservative because the packaging materials above and around the die promotes thermal spreading

thereby increasing the effective heat transfer surface at the case. By increasing the thermal conductivity of the TIM II, lower $Theta_{jc}$ packages may be tested with the embedded thermocouple heat sink. For this study, the silver-filled grease selected as the TIM II material has a reported thermal conductivity of 9 W/m-K. For these calculations, a more conservative estimate of 8W/m-K was used for the TIM II thermal conductivity. A BLT thickness of 50 µm was assumed. Solving for $Theta_{jc} * A_{Die}$ in *Equation (5)* yields an approximation for the critical limit when a heat sink with an embedded thermocouple may be used to measure $Theta_{jc}$.

$$Theta_{jc} * A_{Die} > 125 \frac{C}{W} * mm^2 \quad (5)$$

The error in $Theta_{jc}$ measurements made with a thermocouple inserted in the heat sink is plotted in *Figure 6* as a function of $Theta_{jc} * A_{Die}$. At large $Theta_{jc} * A_{Die}$, the error is less that the 5% target, see for example the CABGA package.

However, when $Theta_{jc} * A_{Die}$ is smaller than 125 C/W*mm², the error becomes quite large. The FCBGA package will require thermocouples mounted into the case.

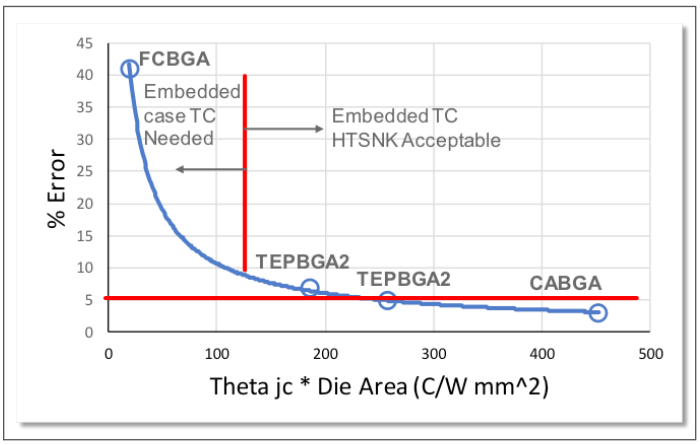


Figure 6. Case measurement method based on $Theta_{jc}$ value.

CONCLUSIONS

The conditions for reproducibility presented here are considered as an initial study in the variability in measurements attributed to the test engineer. The variability in data attributed to the test engineer (as judged by one standard deviation) was approximately 2% of the $Theta_{jc}$ value for most of the packages tested. A more general study of variability would require each test engineer to calibrate temperature sensors, reattach thermocouples, and use their own cooling system. When a high conductivity TIM II material is selected, e.g., silver-filled grease, an embedded thermocouple in a cold plate or CPU cooler may be used to approximate the case temperature if the $Theta_{jc}$ value multiplied by its die area is larger than 125°C/W mm². The FCBGA and higher conductivity TEPBGA2 package required an embedded thermocouple mounted to its case. The lower conductivity TEPBGA2 and the CABGA packages did not require embedded case thermocouples to measure $Theta_{jc}$.

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Beat the Heat in 3D Chip Stacks with Embedded Cooling

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INTRODUCTION

In the Moore's Law race to keep improving computer performance, the IT industry has turned upward, stacking chips like nano-sized 3D skyscrapers. But those stacks, like the law they're challenging, have their limits, due to overheating. A solution to this problem is embedded cooling in which a coolant is made to flow between the stacked high power active layers.

Today, most chips are cooled by fans which push air through heat sinks that sit on top of the packaged chips to carry away excess heat. Advanced water cooling approaches, that are more effective than air-cooling approaches, replace the heat sink with a cold plate that provides more efficient heat transfer. However, because of its electrical conductivity, moving water into a chip stack requires complex isolation measures to protect the chip, and requires impractically large channels to cool large high power die at reasonable pressure drops. The new chip-embedded cooling approach, described in this article, utilizes a benign nonconductive fluid to take this next step of bringing the fluid into the chip (as shown in *Figure 1* below). This does away with the need for a barrier between the chip electrical signals and the fluid. It not only delivers a lower device junction temperature (T_j), but also reduces system size, weight, and power consumption (SWaP).

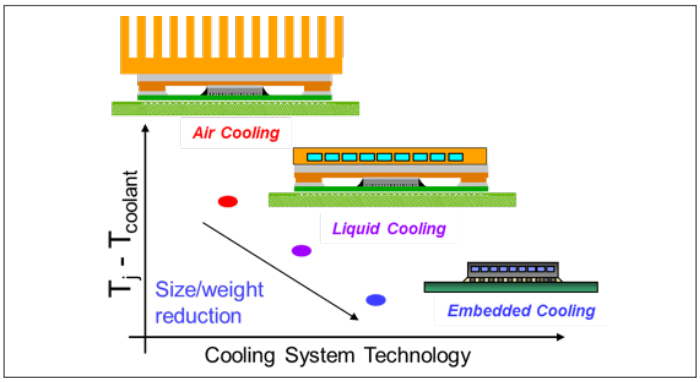

Figure 1. Different types of cooling solution.

This technology provides a solution to cooling 3D chip stacks where a heat sink or cold plate is inadequate for 3D stacking of high power chips because of their inability to cool chips in the middle

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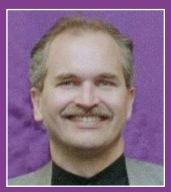

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Dr. Timothy Chainer is a Principal Research Staff Member at the IBM T.J. Watson Research Center and leads a team on Subsystem Cooling and Integration. As Principal Investigator of the IBM DARPA ICECool Fundamentals and Applications programs he led the development of Embedded Two-Phase Cooling for High Performance Computing. He also led programs in system packaging including Principal Investigator for the IBM DOE program on Economizer Based Data Center Liquid Cooling. He is a Senior Member of the IEEE and an elected member of the IBM Academy of Technology. He holds over 200 Patents and has co-authored more than 40 technical papers. Dr. Chainer received his PhD in Low Temperature Experimental Physics from Rutgers University.

and bottom of the stack. This chip-embedded cooling technology circumvents that problem by pumping a heat-extracting dielectric fluid (like the one used in refrigeration systems) into microscopic gaps, some no wider than a single strand of hair (~100 µm), between the chips at any level of the stack. The dielectric fluid used can come into contact with electrical connections, so is not limited to one part of a chip or stack. This ability benefits chip stacks in terms of materials and architecture, such as putting memory and accelerator chips on top of high power chips in the stack, which can improve the speed of everything from graphics rendering to deep learning algorithms [1, 2].

The coolant is pumped into the chips, where it removes the heat from the chip by boiling from liquid-phase to vapor-phase. It then re-condenses, dumping the heat to the ambient environment where the process begins again, as shown in *Figure 2*. As this cooling system doesn't need a compressor, it can operate at much lower power compared to typical refrigeration systems. Key elements of the approach and results are presented in this article, with additional details available in references [1-10].

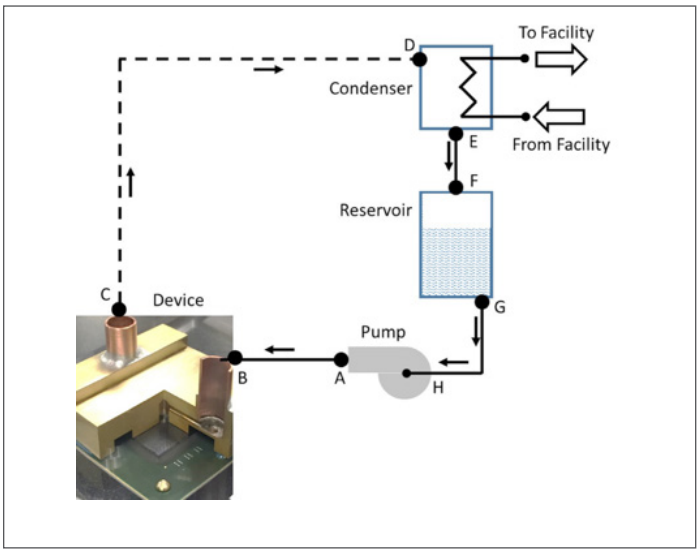

Figure 2. Pumped two-phase cooling loop.

RADIALLY EXPANDING MICRO-CHANNELS WITH MICRO-PIN FINS

Two-phase flow boiling has long been proposed as a potential method for cooling high performance computer systems [11, 12]. A large body of work investigating and developing technologies appropriate for cooling electronics with two phase flow boiling in parallel micro/mini-channels exists [13], but parallel channel two-phase flow is challenged by instability issues, particularly with non-uniform power maps. We utilize a significantly different approach to embedded cooling [3,4]. Rather than moving coolant from one edge of the die to the other through long parallel channels, a dielectric coolant (R1234ze or similar) is fed in at the center of the die, moves through radially expanding channels, and exits at the edges of the die. This approach provides better energy efficiency and maximum critical heat flux with the resulting reduced flow path [4].

The cooling capability was demonstrated on a specially constructed thermal test vehicle (see *Figure 3*) designed to mimic the heat generation capability of real microprocessors without requiring actual transistor based circuitry [3, 10]. In these studies, power densities of 350 W/cm² within an area measuring 3.6 mm x 4.8 mm representing a microprocessor core and 200 µm x 200 µm hot-spot power levels of more than 2 kW/cm² were shown to be effectively cooled.

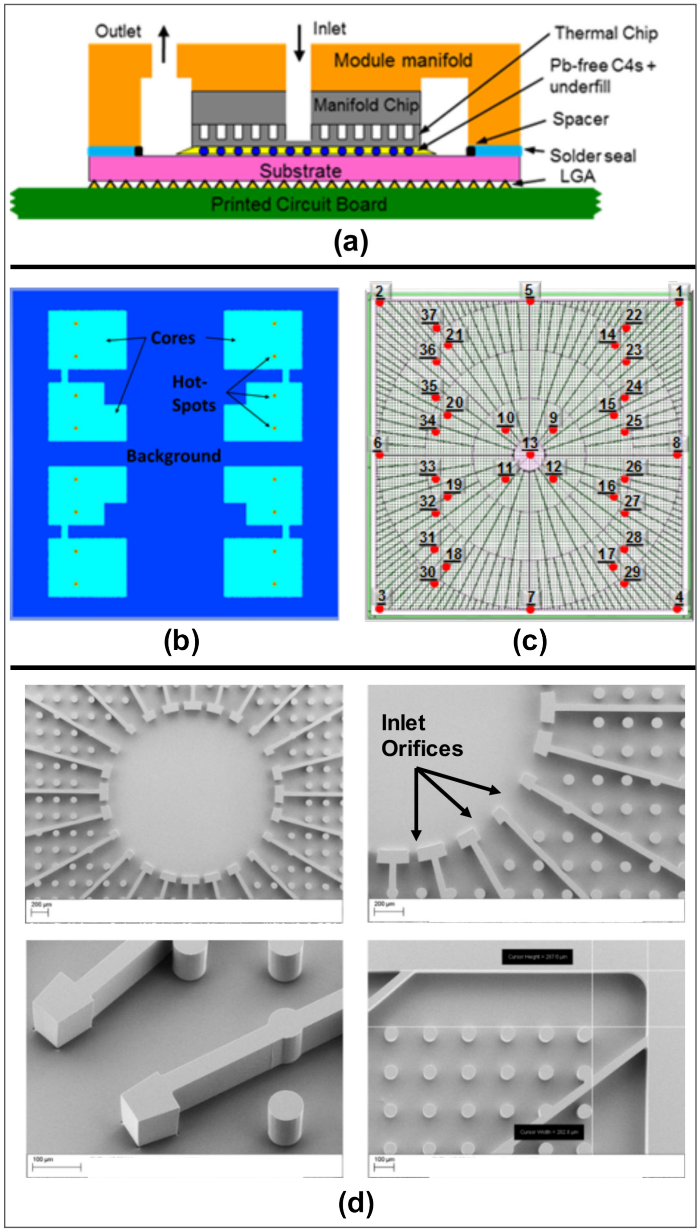

Figure 3. (a) Packaged thermal test vehicle. (b) Representative power map. (c) Relative thermal sensor locations. (d) SEM image of orifices and radial expanding channels.

EMBEDDED TWO-PHASE LIQUID COOLED MICROPROCESSOR (ECM) MODULE

To demonstrate radial embedded two-phase cooling in real devices a commercial two-socket, 2U form factor server was used. The server's 8-core microprocessor modules were modified

into embedded two-phase liquid cooled microprocessor (ECM) modules. Modification of these modules into ECM modules (*Figure 4*) required the creation of an embedded channel design followed by the development of a module fabrication and assembly process. Overall, the embedded cooling structures, including micro-pin field, coolant flow directing walls and orifices, were designed with constraints compatible with future 3D structures, which would include through silicon vias (TSVs). To modify the microprocessor module for embedded cooling the lid, seal and thermal interface material were removed to expose the processor die. A deep reactive ion etch (DRIE) of the processor die was performed to generate the 120 µm deep cooling channels structures (*Figure 4(c)*) on the backside of the processor die. Next, a glass die was bonded to the etched processor die to create the top wall of the micro-channels. Finally, a brass manifold lid, which provides for coolant supply and return, was bonded to the glass manifold die and the organic substrate using an adhesive. The ECM module was placed in a commercial server, as shown in *Figure 4(d)*. Additional detail on the ECM module design and fabrication process can be found in Schultz et al. [8, 9].

The coolant (R1234ze) enters the ECM module and passes through 24 inlet orifices to distribute the flow among the corresponding 24 radial expanding channels (6 per quadrant). A combination of detailed full-physics [14] and reduced-physics models [15] was used to model the two-phase flow and heat transfer process to design and optimize the cooling channels structures including the central inlet diameter, dimensions of inlet orifices and number of radial expanding channels. The coolant removes heat from the chip as it flows through the radial expanding channels and transitions from liquid phase to vapor phase before exiting the ECM module as a liquid-vapor mixture. The coolant delivery to and return from the ECM module is controlled by the test system shown in *Figure 2*. The condenser connected downstream of the ECM module, extracts the heat from the exiting liquid-vapor mixture and condenses the vapor back to liquid. The liquid coolant then flows into the reservoir and is pumped back to the ECM module.

It is of interest to compare the performance of ECM modules with their baseline air-cooled state. Shown in *Figure 5(a)* is the before (air-cooled) and after (two-phase liquid cooled) comparison of average cores temperature for two ECM modules. The cores temperature was measured using 40 (5 per core) on-chip digital thermal sensors [9]. Coolant inlet temperature in both cases is 25 °C. The dielectric coolant mass flow rate is 9 kg/hr at a pressure drop of 75 kPa (~11 psi) which, for a pump efficiency of 0.1 results in ~1.5 W of coolant pumping power. The improvement in operating temperature is substantial. Note that the air-cooled curve levels off at around 70 °C as the system fans speed up (~65%) to prevent overheating [1]. At the highest power operation (4.3 GHz) the reduced operating temperature results in over a 10 watt decrease in the power consumed by the microprocessor along with a significant reduction in fan power (15+W) that would be concomitant with such a system [9].

Shown in *Figure 5(b)* is pressure drop versus flow rate data for an ECM module at three power levels. While there is an observable increase in pressure drop at full power, it is still relatively small. Therefore a coolant supply system utilizing a relatively simple "pump-on" operating mode, without flow or pressure control, would have relatively minor changes in flow and/or pressure drop with changes in operational power level. This also implies that modules could conceivably be operated in parallel without active flow balancing between modules when module power levels change. In all cases, the observed pressure drop was quite stable, with no evidence of flow instability.

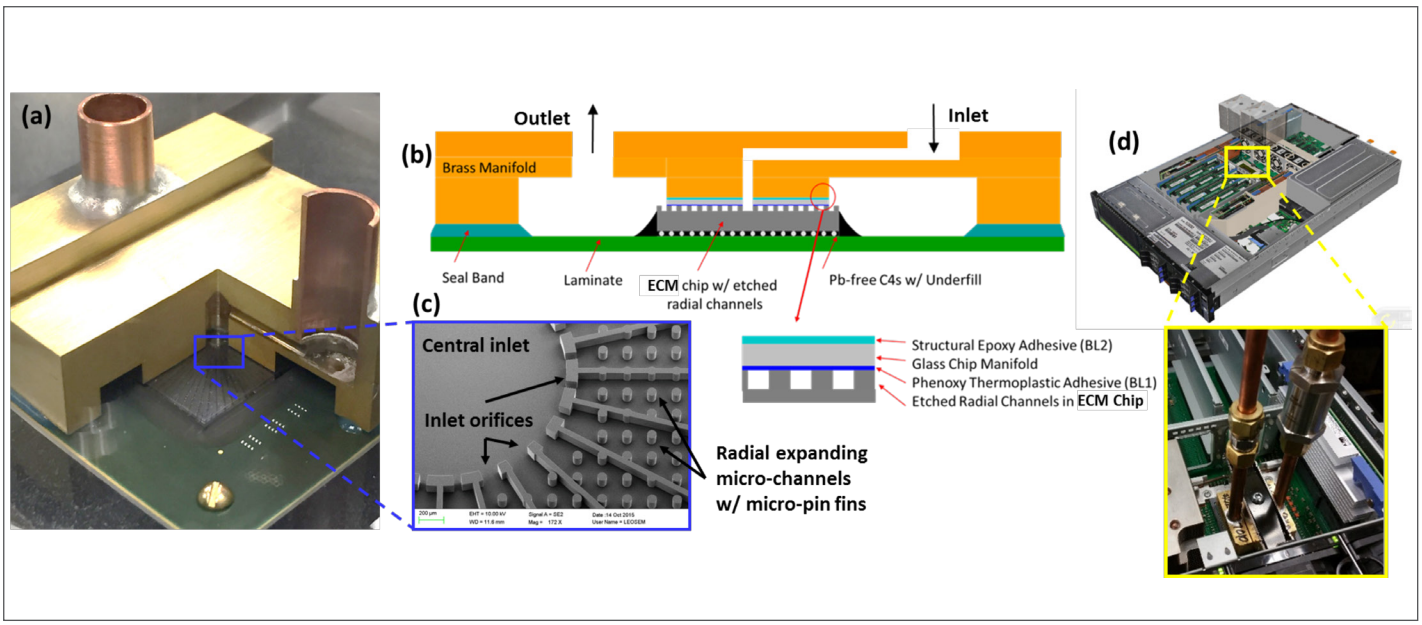

Figure 4. (a) Cut-away view and (b) cross-sectional view of the ECM module. (c) SEM image of cooling channel structures. (d) ECM installed in a commercial server.

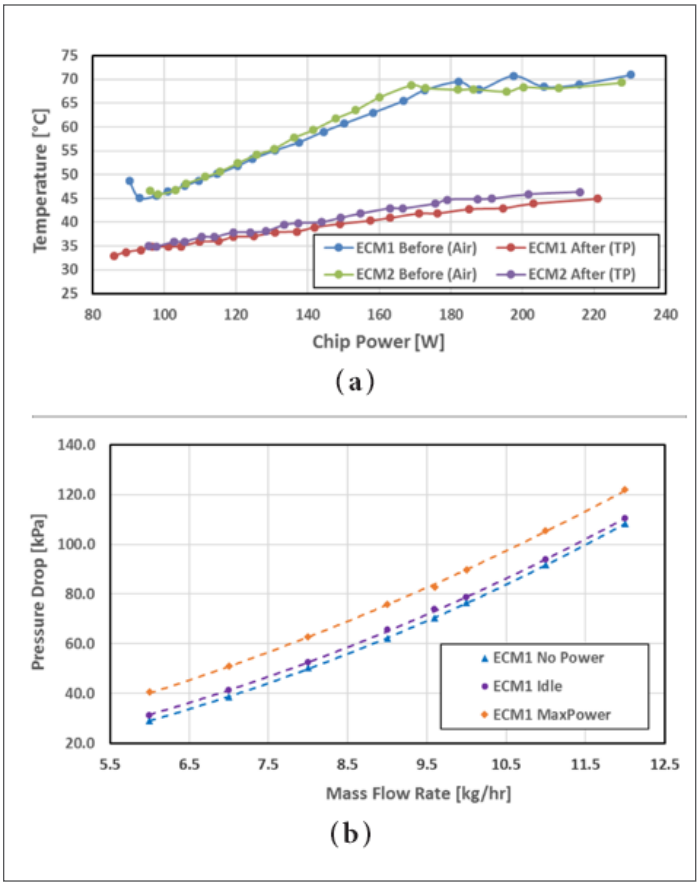

Figure 5(a). Before and after-modification comparison of average core temperature at different power levels for two ECM modules. (b) Pressure drop vs. mass flow rate for an ECM module at three different power levels.

THERMAL MODELING AND VALIDATION

The development of an embedded two-phase cooling solution requires a comprehensive understanding to design the various constituent sub-components such as inlet orifices, two-phase flow in micro-channels, two-phase flow through micro-pin-fin arrays oriented at arbitrary angles relative to the flow direction, etc. A key challenge is to develop high fidelity conjugate thermal models of the chip-package having spatially varying, and workload-, temperature-, and operating frequency-dependent heat sources together with a two-phase microfluidic convection network. This includes integrating together the variations in coolant saturation temperature, local heat transfer rates, friction coefficients, and vapor quality along with complex thermal conduction in the microprocessor package.

We have developed a novel Hybrid Thermal Model (HTM) that uses characteristic features of both reduced-physics and full-physics models, and integrated that with an electrical model of the microprocessor for fast and accurate prediction of thermal behavior of an embedded two-phase liquid cooled high power electronic devices. A comparison of the junction temperature prediction by the HTM against the on-chip digital thermal sensor data for an ECM module demonstrates the model accuracy (see *Figure 6*). Further details have been published [5, 6].

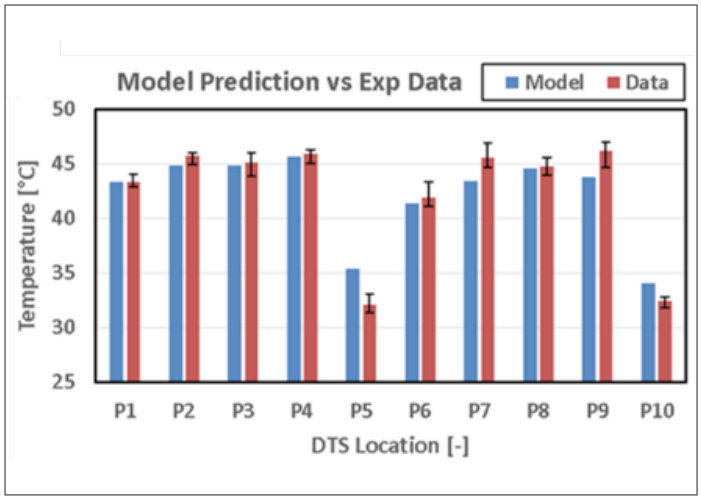

Figure 6. Comparison of chip temperature prediction by HTM against the on-chip digital thermal sensor data for an ECM module.

CONCLUSION

Advanced thermal solutions provide three major benefits to computer efficiency. First, integration of liquid cooling into the chip reduces chip junction temperature and leakage power, which lowers the energy per computation. Embedded two-phase cooling of microprocessor modules demonstrated junction temperature reduction by 25 °C, and chip power usage reduction by 7 percent compared to traditional air cooling. Second, chip-embedded cooling reduces the thermal resistance between the chip and the coolant allowing coolant temperatures above the outdoor ambient temperature, thus eliminating sub-ambient energy intensive cooling requirements. Finally, the integration of chip stack embedded liquid cooling provides a path to high bandwidth 3D chip stacking of heterogeneous components, which has the potential for computational performance improvements.

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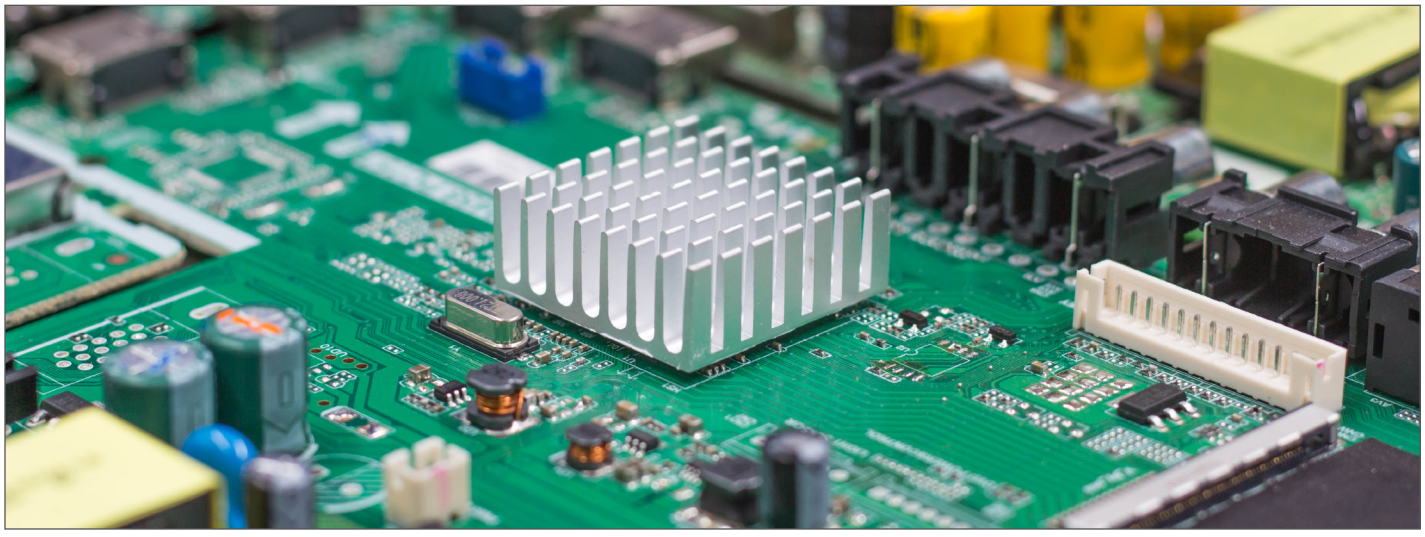


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Strategies for Using Thermal Calculation Methods

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Thermal analysis tools available to engineers and scientists offer a wide variety of methods to solve problems. A cursory review of the past decade's issues of *ElectronicsCooling* magazine can show methods ranging from analytical techniques (such as hand calculations) to spreadsheets to full numerical/computational solutions such as CFD (Computational Fluid Dynamics) and FEA (Finite Element Analysis).

Although articles have discussed important basics such as how to use a particular method, and what to do to ensure sound results, the present authors note the issues of when or where to use any particular method have not been discussed as thoroughly. A few articles in the literature have partially addressed this (see [1]-[2]). Often thermal engineers do use a method appropriate to the problem, but as a group default to a method or technique that is comfortable and familiar. A better solution method may be available but not considered because of this bias. Due to this normal characteristic of human behavior, it is time for a careful examination of the methods available today, and for strategically using different methods (the when or where of the method, which means understanding the underlying why one method may be best).

CLASSIFICATION OF PROBLEM

The best place to begin deciding what type (or multiple types) of solution method may be preferred is to classify the problem to be solved. The two classification methods used for this article will be examining the geometry definition of the problem and the goals of the thermal model.

This means understanding two things clearly: what type of information is available at the problem definition; and the end goals of the solution. Examining these two areas will tend to point one in a specific direction. They also will point out the possibility of other solution methods and the advantages they may contain over one's typical method.

Geometry definition is a statement about how much detail about the geometry is known at the time the problem is to be solved. Anyone who has been involved in a variety and significant number of projects has seen a wide range in this category. Often thermal analysts have been brought in late to solve an issue after the entire project is nearly complete; in these cases the geometry is well defined and often thoroughly detailed in explicit CAD models with complete bills of materials. One could label these as "fully defined" geometry definitions.

Sometimes thermal issues are addressed early in a design process, and in these cases very little may be explicitly defined. The analyst may know there will be some number of PCBs, and that the overall product dimensions will be about x by y by z, and that the enclosure will have certain features typical of the product class, but perhaps little is known beyond that. The thermal dissipation may even be only roughly known and may have a wide possible range owing to product features being not well defined. Such a situation could be described as a "nebulous" geometry definition, or architecture phase.

Certainly some combination of the "fully defined" and "nebulous" cases exist, and often this is found in many design situations. Perhaps the PCB is an existing item and will be reused in a new product, so it is well defined while the remaining design around it is mostly unknown. This condition will be labeled as the "partially defined" geometry definition.

All three of these conditions encompass the full range of geometry definitions one may find when beginning a thermal analysis, and as the authors explain, it is beneficial to consider the starting point when making a choice of tool for the analysis.

The second problem classification revolves around the goals of the thermal model. These may change over time. The thermal model goal typically falls into one of two broad categories.

The first goal category could be called the multiple-scenario or design trade-off study. In this situation, there may be several types of solutions that could be used to solve the thermal problem. Each type of solution may be quite different from other ones in geometry, material or type of cooling system. Changes to design strategies or thermal paths may be significant among the options. Adopting a particular solution in one design may involve a trade-

off with other desirable features from another.

For example, one could examine a product that is a chassis with internal electronics. Perhaps the design could be cooled by natural convection; this requires a certain surface area and possible ventilation openings. Care would be required to place heat sinks, components, etc., in the appropriate places for cooling. Touch temperatures may also need to be considered. The same product could also be cooled by forced convection. In this case, fan placement, air inlet and outlet sizes, and noise requirements all must be evaluated. The installation of the product in its environment also factors into the product solution; blowing hot exhaust air onto an end user would not be suitable for most products. Other variables besides these can also be important, but this example shows that some thermal modeling goals may have numerous starting points. Ultimately this type of problem requires evaluating many geometries and finding the thermal performance of each one.

A second goal category could be called fully specified. In this case, there are few types of solutions to examine, but they are detailed designs. This is common in later project phases when a particular solution has been chosen. While chassis designs and layouts may be close to final form, some smaller details may be undecided, such as type and placements of thermal interfaces, heat sink fin spacing, effect of gap pads, or rearrangement of PCB hot components. Once a product final design is completed, a final thermal analysis is often performed as part of the product launch verification, and would also fit this category.

SOLUTION METHODS FOR PROBLEM CLASSES

With these classifications and goals in mind, one can then examine the solution methods available and see that there are some reasonable fits between the problem and type of solution method. This is an important step. One mistake people tend to make is to use and re-use methods they are most familiar with rather than what may be most suitable. This leads to forcing a method or tool to solve the problem. While this will still lead to solutions, it is not necessarily the best manner to go about this process. From this viewpoint, the authors propose the following matches of methods to the problem classes previously described:

Numerical Analysis with Systems of Fundamental Equations for Nebulous Geometry or Multiple Scenarios

When geometry is largely unknown, or multiple scenarios must be evaluated, it is most efficient to keep factors set to a variable or numerical value to allow for faster changes. For example, the convective surface area of an enclosure could be represented by a number (say 0.25 m^2), or it could be explicitly modeled in 3D CAD. If one wished to change this area to 0.3 m^2, this is an easy change if it is just a variable in an equation; the change becomes much harder if the 3D model must be changed (and this becomes cumbersome if several variables have a number of values to be evaluated).

To use this method, systems of fundamental, simultaneous equations are written and solved. In the authors' experience this is tractable if the number of equations and unknowns is under 25 or so; beyond that may be difficult to set up and solve effectively, depending on the solution algorithm. The equations are forms of the three basic heat transfer equations for conduction, convection and radiation familiar to the reader:

$$kA = l(T_1 - T_2)$$
$$Q = hA(T_1 - T_2)$$
$$Q = \sigma A f \varepsilon (T_1^4 - T_2^4)$$

A key point here is that the heat flow path must be visualized enough to write the equations correctly. The visualization exercise is an extremely powerful thought and discussion tool. The solved equations serve to quantify the relative heat flow paths, identifying trouble spots and opportunities for improvement. Of course, the accuracy of the results depends heavily on the accuracy of the thermal network. Sometimes several versions of the network are needed to arrive at a suitable representation — just as several versions of experimental or computational models are needed to achieve confidence in the model. Also, sometimes the accuracy of the solution is less important than the ability to quantify relative effects in order to make a good design decision. For the design decision, the ability of the network to capture the effect of a design variation is key.

Given a suitable range for the average of the outer shell temperature:

$30\,°C \le Tshell \le 70\,°C$

$$Qrad = \sigma \cdot f \cdot em \cdot A_{ext} \cdot \left(Tshell^4 - T_a^4\right)$$

$$Qnc\_ext = h_{nc} \cdot A_{ext} \cdot \left(Tshell - T_a\right)$$

$$Qnc\_int = Qnc1 + Qnc2$$

$$Qnc1 = h_{nc} \cdot A_{int\_shell} \cdot \left(Tshell - T_a\right)$$

$$Qnc2 = h_{nc} \cdot A_{int\_horiz} \cdot \left(Thoriz - \frac{2T_a}{2}\right)$$

$$Q_{Th} = Qrad + Qnc\_ext + Qnc\_int$$

$$Qrad = k_{graf} \cdot \frac{A_{graf}}{L_{graf}} \cdot (Thoriz - Tshell) - Qnc1 - Qnc\_ext$$

$$\frac{h_{nc} \cdot L1}{k_f} = 1.05 \cdot \left[\frac{c_p \cdot \mu_f}{k_f} \cdot \frac{gr \cdot \beta \cdot \rho_f^2 \cdot L1^3 \cdot \left(Tshell - T_a\right)}{\mu_f^2}\right]^{.215}$$

$$Qnc\_int = Coeff \cdot A_{int\_airflow} \cdot \left(\frac{Tout - T_a}{Tout + T_a}\right) \cdot \left[\left(\frac{Ht}{X}\right) \cdot \left[\left(\frac{Tout}{T_a}\right) - 1\right]\right]^{0.5}$$

Figure 1. Sample fundamental equation network [5].

To solve the system of equations, software that is essentially high level programming (e.g., commercial codes such as MATLAB or Mathcad, or network solvers such as the SPICE codes for solutions) is well suited to the analytical method. *Figure 1* shows a sample problem set up using Mathcad. Author Petroski has used this method for small electronic devices dissipating a few watts to much larger electronic cabinets of 1kW dissipation with good correlation to product tests.

The network equations can also be implemented in spreadsheet form if needed, see [4]. There are many powerful programming tools available in spreadsheets far beyond simply coding formulas using cell references with row and column indicators. The biggest advantage of spreadsheet analysis is that the software is available on nearly every computer as part of an office software suite, requiring no additional purchase or installation. This feature facilitates sharing and discussion with team members who are not thermal specialists. A disadvantage of solving the network equations in a spreadsheet is that the solution equations must be coded afresh if there are changes in number of nodes, or in the way they are linked together. Also, since everything is done manually, debugging and assessing the suitability of the network are entirely up to the user. Another disadvantage to spreadsheets is that non-linearity in the equations (for example, properties that depend on temperature) can be tricky to handle, although there are ways to include these effects that are beyond the scope of this article.

Numerical Analysis with Discretization for Nebulous Geometry or Multiple Scenarios

Solving the same type of problem as the previous case is possible with a resistance network that would discretize the model into more regions. It also may allow for easier solutions with other programming methods; some non-linear areas of a problem may be translated into linear forms without much loss of fidelity. For example, a flat plate with a small heat source may contain spreading resistances; such a problem may be handled by discretizing the region into smaller regions with the appropriate conduction equations (see [3] for such equations). Such a problem could allow for multiple spreading scenarios to be examined without using a single equation for spreading and possibly violating its assumptions. Viewed another way, perhaps a design may or may not incorporate spreading as a significant contribution to the heat transfer. A discretized region that can incorporate spreading, or not, by using the conduction equations may simplify solving the model for a variety of materials and geometries.

For this method, solutions can be found with many of the same network solution techniques described in the previous section. Another class of solvers known as finite difference solvers can be used and thermal versions of such programs (SINDA is a well-known example) provide the advantage of thermal resistance elements for each type of heat transfer, along with debugging and solution assessment.

Hybrid Solutions for Partially Known Geometry and Some Trade-Off Studies

When some of a problem's geometry is well-defined, a combination of a fully discretized solution and some ability to handle unknown geometry is useful. For example, one may have a PCB or electronics module whose design is complete, but whose surrounding chassis or enclosure design is not defined. The two previous methods work well for the unknown area of the design where single or small numbers of nodes represent major sections of it. A well-defined numerical model can be used for the known module.

These two types of models then need to be combined for a solution. With the proper heat transfer equations one can connect these two parts. Perhaps the simplest manner to model this is to use the finite difference modeler. A discretized model is feasible for the well-defined portion of the model, and simple thermal resistance elements make up the connections to the undefined areas and the undefined geometry as well. As an example, see *Figure 2.* A portion of the model is well discretized and defined, while the rest of the model is composed of few elements. Model creation, with the solutions for different scenarios, is a straightforward process. The flexibility this approach provides for the unknown geometry is useful to find a final design that should meet the system temperature requirements, while providing good fidelity for the known geometry thermal profile.

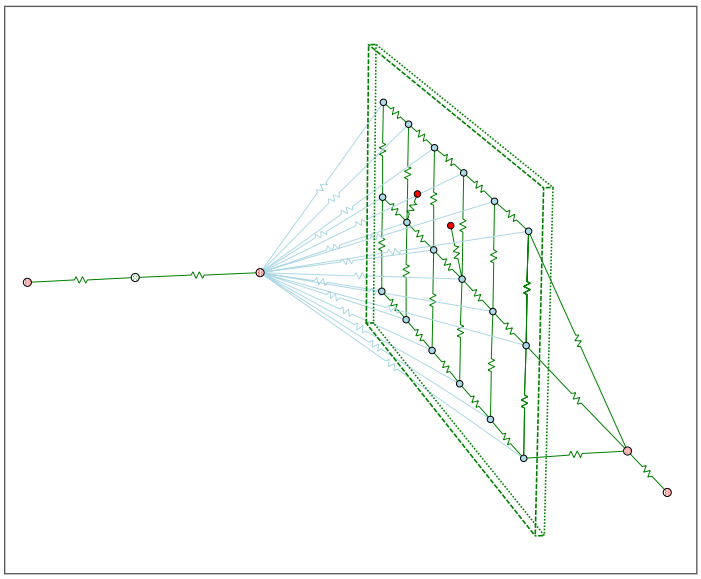

Figure 2. Sample hybrid network in a finite difference modeler [6].

Automated Numerical Solutions for Fully Defined Geometry and Fully Specified Goals

The final case is where the geometry of the problem is fully defined. This occurs near the end of the development when full CAD-based geometry is complete. At this point, a fully automated numerical solution is feasible with a complete discretized grid or mesh and appropriate boundary conditions, material properties,

thermal loads, etc., applied. Any of the commercial or academic codes from the finite element method, computational fluid dynamics or the finite difference method can be used for this solution type. For this solution, the goal is often a final or near-final analysis of the problem and iterations for geometry changes or different scenarios are usually few or none. The greatest detailed solution is found with this method, but at the cost of knowing the final design and often is the longest solution time.

CONCLUSIONS

There are several methods to solve any thermal analysis, but given the different levels of geometry definition one can face, and the different types of goals for the end analysis, it is best to choose a solution appropriate for the class of the problem. Different solution methods have different advantages, and one should choose a method best compatible with the end goal(s). Ideally one should choose a solution method that provides the best efficiency for the type of problem at hand. This will assist in avoiding approaches that resemble the proverb, "If you only own a hammer, everything looks like a nail." CFD is a fine problem solver, but if one is looking to evaluate multiple scenarios and many geometric conditions, a situation where dozens of analyses may result in weeks passing before everything is evaluated where another modeling approach would complete the task in hours or a few days.

Another drawback of using CFD directly is that fundamental limitations to the problem aren't flagged, whereas the thought process required by model construction forces identification of the limiting factors. Thus, evaluating the basics first is also important — one could do a lot of modeling, only to find that the constraints are infeasible. This leaves the engineer doing a great deal of work with no result or poor results, and may be likened to using a hammer to pound in a screw, to alter the proverb. Simpler methods often identify important features and point to the solutions without resorting to extensive modeling.

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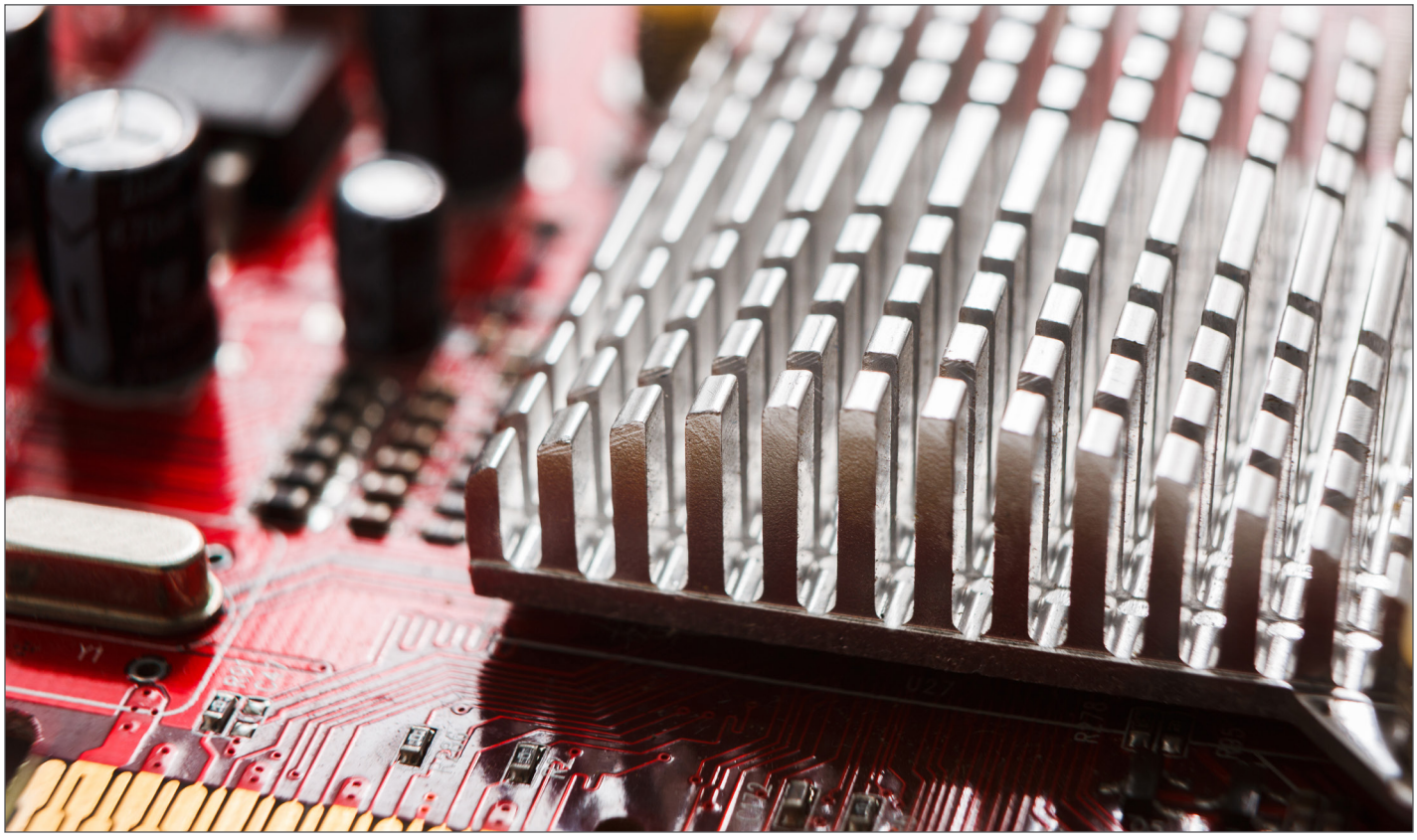

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