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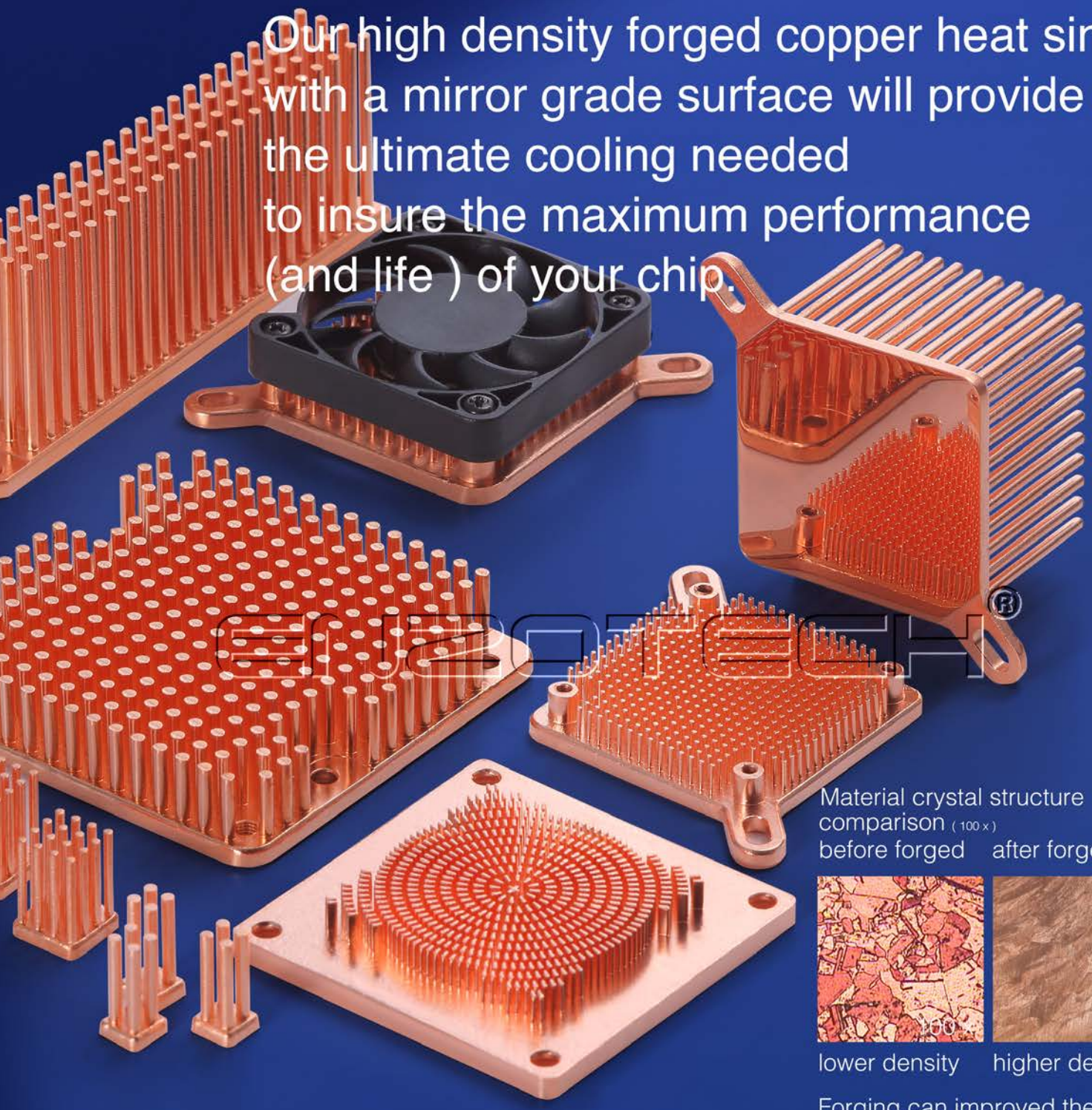

Material crystal structure comparison (100 x)

before forged

lower density

after forged

higher density

Forging can improved thermal conductivity 5-10% on average

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EDITORIAL

Bruce Guenin
Associate Technical Editor

In Praise of Thermal Standards

Looking back over the last few decades, we've seen amazing advances in chip functionality as enabled by Moore's law scaling—shrinking CMOS gate size, reduced gate power, increased operating frequencies, and more input/output channels operating at higher bandwidth for data exchange with other devices. These developments, at the chip level, have enabled proportional increases in the performance of individual servers, which, in turn, have propagated to the data center level.

This accomplishment is noteworthy in its own right. It becomes even more so when one figures that the technical developments that made these advances possible involved thousands of different companies, each operating within its own technical niche, but with their collective efforts having enough coherence that the entire enterprise can function amazingly well.

What contributes to this coherence even between competing companies? Many of the company-to-company interactions are confidential, involving the exchange of proprietary information. However, the industry long ago decided that it was to the mutual benefit of competitors in a particular sector of the industry to cooperate through the development and promotion of numerous industry standards of every type imaginable, including, of course, thermal standards.

In this issue, we are pleased to have two articles, each providing an update from the one of the chairmen of the two leading thermal standards organizations, that have played an important role in promoting the development and application of best practices in thermal engineering and disseminating them throughout our industry. These committees are: the JEDEC JC-15 Thermal Standards Committee, chaired by Dr. Jesse Galloway, dealing with chip- and package-level standards; and the ASHRAE Technical Committee 9.9, Chaired by Dr. Dustin Demetriou, developing standards at the server and data center level.

We owe a debt of gratitude to both of these committees, since they face many challenges in fulfilling their respective missions. They must ensure that the scope of their body of standards continually expands to keep up with the constant steam of technical developments in the industry. Even after that is done, they still have to document the standards in a manner that makes them understandable to a diverse, world-wide community of engineers, representing many different levels of expertise.

The above efforts on the part of committee chairmen and members must appear to be rather daunting to much of our readership. However, I can assure you, on the basis of my own experience as a past Chairman of the JC-15 committee, that the rewards of participation are also great. There is abundant satisfaction in seeing a standard that one has contributed to, released to the industry, and having an impact on engineering as it is practiced in the real world. It also represents a great learning experience as committee members collectively explore the trade-offs inherent in the implementation of different technical strategies. The level of detail and nuance in these discussions can often be quite extraordinary. Also, these discussions are often accompanied by a sense of urgency as the participants realize that higher quality standards ultimately benefit the end users and make their jobs easier.

I encourage all of our readers to consider joining a standards committee that best suits their expertise. I'm sure that Drs. Galloway and Demetriou would enjoy learning of your interest.

- Bruce Guenin

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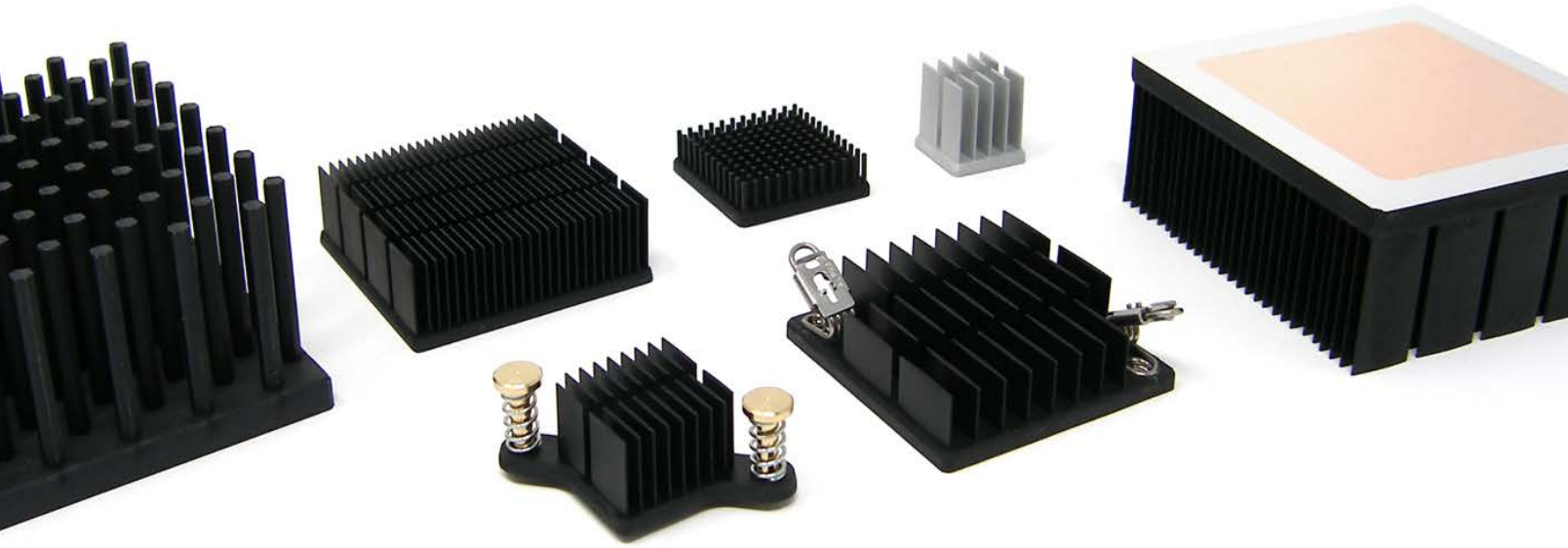
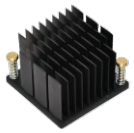



Tabbed Push Pin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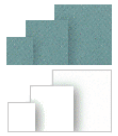
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COOLING EVENTS

News of Upcoming 2019 & 2020 Thermal Management Events

12TH FKFS-CONFERENCE: 'PROGRESS IN VEHICLE AERODYNAMICS AND THERMAL MANAGEMENT'

Haus der Wirtschaft, Willi-Bleicher-Straße 19, 70174 Stuttgart, DE

The FKFS-Conference is an ideal location to get latest information about new car developments, new or improved testing techniques and new or improved calculation procedures. It is an ideal forum to meet leading experts from industry, universities, and other institutions, to exchange ideas and discuss new ones. Furthermore, demonstrations will show state-of-the-art measurement technology applied live in FKFS Wind Tunnels and Laboratories.

► http://fkfs-veranstaltungen.de/index.php?id=143

MWC LOS ANGELES 2019

Los Angeles Convention Center, Los Angeles, California, USA

Welcome to the era of Intelligent Connectivity—where speed, convenience, and intelligence converge; inspiring new technologies that keep us connected to everything and everyone, while delivering highly contextualized and personalized experiences, when and where you want them.

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In 2019, the workshop is being held at the Microsoft Corporation Conference Center on the Microsoft headquarters campus, near Seattle WA. This new venue allows us to expand the number of attendees and number of technical exhibits.

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See pages 42 – 43 for Semi-Therm's® 2020 Technical Program. For program details, registration, exhibition and hotel information, please visit:

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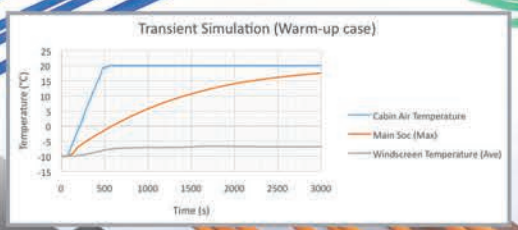

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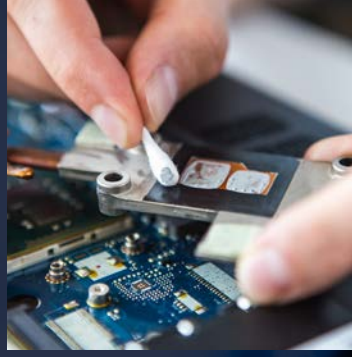

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THERMAL LIVE™ 2019 TECHNICAL PROGRAM

OCTOBER 22 – 23, 2019

TUESDAY | OCTOBER 22, 2019

BRUCE GUENIN, Ph.D. | 9:00 am ET

Associate Technical Editor, Electronics Cooling®

Keynote: Whatever Happened to the Predicted Data Center Energy Consumption Apocalypse?

In the early years of the internet between 2000 and 2008, the total energy consumed by data centers in the US increased by 15% per year, representing a doubling of energy consumption in six years and a tripling in nine years. This created a sense of urgency leading to very pessimistic projections about future energy consumption by data centers that persist even to today. The reality is actually quite different, with data center energy consumption increasing at a modest rate of less than 2% per year since 2008. This presentation examines the effect of Moore's Law scaling in improving the inherent energy efficiency of computer, storage, and networking hardware. It also explores the structural changes in the IT industry in which high-end and hyperscale data centers, with state-of-the-art energy-efficient technologies, produce an increasing fraction of the total IT workload in the US.

TIM JENSEN | 10:15 am ET

Senior Product Manager for Engineered Solder Materials, Indium Corporation

Liquid Metal Thermal Interface Material Innovations for High-Performance Devices

The idea of using liquid metals as a thermal interface material (TIM) is not new. Liquid metal provides very high thermal conductivity, as well as low interfacial resistance when in contact with most surfaces; however, there have always been a number of material and process challenges that limited their adoption. This presentation with review those challenges while discussing liquid metal material innovations that enable higher performance as compared to conventional TIMs.

NICOLAS MONNIER | 11:15 am ET

Product & Marketing Specialist, Stäubli North America

Product Demo: Design Consideration for the Mechanical Integration of Quick Disconnects in Liquid Cooled Electronic Systems

Liquid cooling for heat dissipation in electronic systems is becoming a requirement as the power of components is increasing, as well as density. The use of performant quick disconnects allowing the hot swap of the active components from the static structure is understood and embraced by the thermal community. As theory becomes practice, it becomes the responsibility of the mechanical engineer to integrate that component reliably. The presentation will go over some of the mechanical and practical solutions proposed to interface with the system architecture. These must be considered at the early stage of the global design. Their proper integration will influence the reliability of the liquid line as well as the total cost of the system.

TUESDAY | OCTOBER 22, 2019 | *CONTINUED*

DANNY LEONG | 12:00 pm ET

Principal Application Engineer, Technical Customer Service, Henkel

Raising Reliability of Devices for 5G Telecom Infrastructure

The coming era of 5G mobile communications has users excited about the possibilities and broadband systems designers and manufacturers a bit nervous about the realities. While handheld devices may have the required chipsets, infrastructures must be able to manage the huge amounts of data and speeds required to satisfy 5G demands. Reliable 5G networks will clearly require a host of solutions – at the printed circuit board level all the way up to the final system enclosure – to deliver on the huge expectations. Keeping all systems go also means keeping all systems cool, making thermal management one of the most critical pieces of the 5G solution. Henkel's has recently launched BERGQUIST® GAP PAD® ultra-low modulus portfolio especially in this 5G telecom infrastructure application.

CHRISTIAN MIRAGLIA | 1:15 pm ET

Applications Engineering Manager, Fujipoly

Understanding Thermal Gap Filler Pads, PCB Deflection and Stress

Managing compression force and stress is critical in any application that incorporates gap filler pads as a thermal interface. In this webinar we will look at the compression characteristics of thermal gap filler pads. We will apply this understanding to a PCB assembly. Webinar attendees will have a better understanding of what basic analytical techniques and tests can be performed to understand stress as well as defection in both gap filler pads and PCB.

WEDNESDAY | OCTOBER 23, 2019

JEFF PETERS | 12:00 pm ET

Project Manager, Thermal Management, CPC (Colder Products Company)

The Future is Now: Advanced Connector Solutions for Liquid Cooling

CPC, a global leader in QDs for liquid cooling applications, will cover key thermal engineering factors to consider in specifying QDs in liquid cooling systems. Jeff Peters, mechanical engineer and CPC thermal management product manager, will describe the evolution and characteristics of various connector options for a range of applications as well as provide comprehensive information about the future of QDs—engineered polymers. Just coming to market, advanced thermoplastic QDs are lighter-weight alternatives to stainless steel and meet or exceed requirements for thermal performance, chemical compatibility, anti-corrosion and condensation management, and long-term, leak-free operation.

THERMAL LIVE™ 2019 TECHNICAL PROGRAM

OCTOBER 22 – 23, 2019

WEDNESDAY | OCTOBER 23, 2019 | *CONTINUED*

KIMBERLY FIKSE | SPEAKER | 1:15 pm ET

Applications Engineer, ACT (Advanced Cooling Technologies)

ANDY SLIPPEY | Q & A MODERATOR

Product Development Engineer, II ACT (Advanced Cooling Technologies)

Passive and Active Two-Phase Cooling for Power Electronics

Advanced Cooling Technologies will review strategies for managing the rising waste heats from Mosfets, IGBTs and other Power Electronics modules using two-phase technology. This session will focus on loop thermosyphon and pumped two-phase (P2P) solutions. Both technologies provide high thermal capacity, while also provide unique benefits to power electronics, such as dielectric working fluids and packaging flexibility. Please join us to review theory and practical applications for these emerging technologies.

BRANDON NOSKA | 3:00 pm ET

Sheetak

Advancements in Solid-State Cooling Technologies

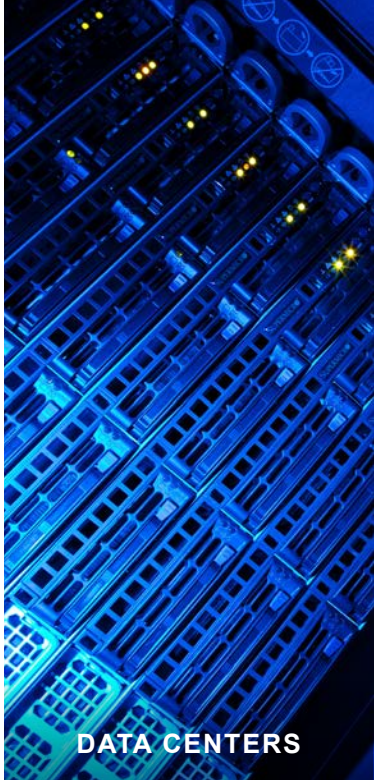
This presentation will cover market trends driving the need for increased efficiency and miniaturization of solid-state cooling technologies. We will show different device architectures to achieve higher temperature differentials with increased COP. In addition, we will describe a novel thin film cooling technology platform to enable more efficient, higher performance micro coolers for a broad spectrum of optoelectronics and other electronics applications.

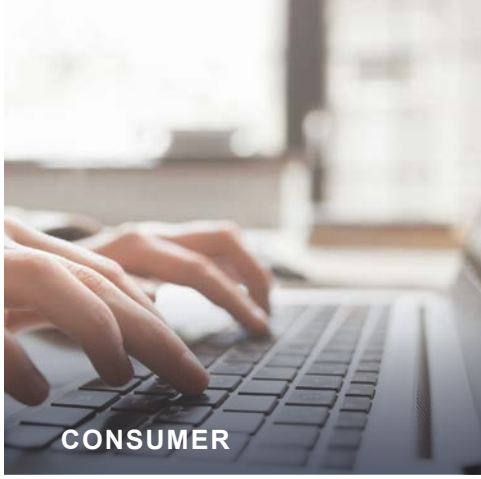
ANANTH SRIDHAR | 4:15 pm ET

Applications Engineer, OnScale

Next-Generation Electronics Packaging Design with OnScale Cloud Engineering Simulation

In this presentation, we describe how OnScale supports efficient solutions to highly complex design issues in Electronics Packaging with its highly parallelized proprietary multiphysics solvers on the Cloud. Further, we demonstrate how OnScale's revolutionary platform lends itself for multi-objective multi-variable optimizations studies of advanced package designs including 1000s of models that can be run at a fraction of time and cost compared to legacy simulation software.





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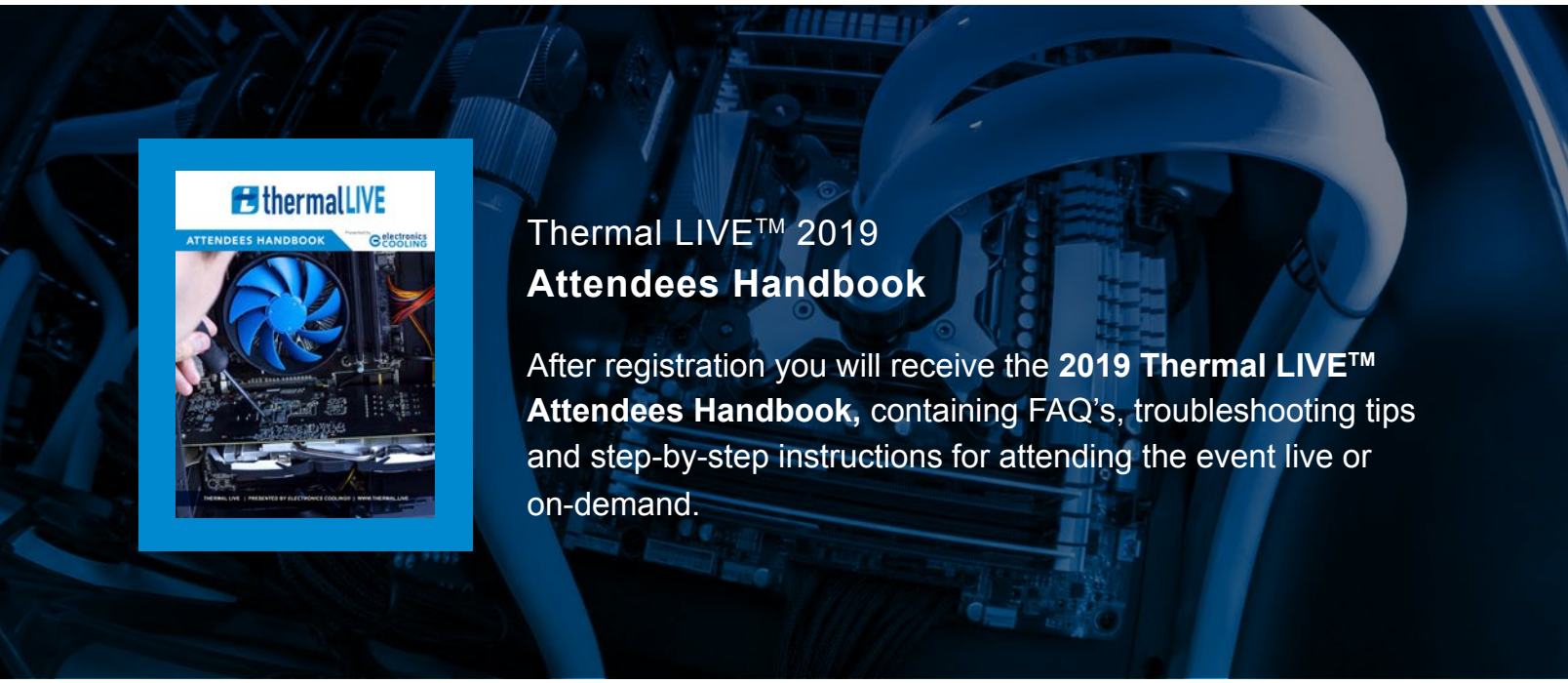

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- Foster discussions between thermal engineers, professionals and industry experts
- Encourage the exchange of information on academic and industrial advances in electronics cooling

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Manuscripts and extended abstracts submission deadline	Date that authors are notified of acceptance	Photo-ready full manuscript submission due date
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Larger Errors with Smaller Stuff

Ross Wilcoxon
Associate Technical Editor

Long time readers of Electronics Cooling® will undoubtedly recall one of our former editors: Clemens Lasance. One of Clemens' many contributions to the magazine was the creation of the original "*Thermal Facts and Fairy Tales*" column, which provided a forum for him to discuss a variety of issues related to the use and misuse of information related to the topic of electronics cooling and thermal management. I have known Clemens for many years, and I feel confident that when I describe him as "willing to say what he thinks," it is unlikely to provoke an argument from other people who know him. One topic that Clemens has always been willing to express an opinion on is the use of empirical correlations in engineering analysis.

In a number of Electronics Cooling® articles, Clemens outlined his many concerns regarding the use of empirical correlations. One of these concerns included the fact that, even with the simple geometry of a flat plate with natural convection, correlations developed by different researchers for the same geometry can vary by 100% [1]. He was also pointed out that the incorrect use of non-dimensional parameters can lead to correlations that do not exist. For example, if a given configuration is tested with a wide range of the critical length scale (such as diameter), the Nusselt number will increase with Reynolds number even if the convection coefficient is constant [2]. Another concern was with the use of correlations developed for simple geometries, such as flow channels, for estimating the performance of more complex systems such as flat plate heat sinks. The pressure drop of a heat sink estimated using different correlation approaches was as much as twice the value determined with experiments [3]. The general conclusions from [1-3] can be summarized as "geometrically and physically complex phenomena cannot be described by simple equations" [2].

An additional concern with using correlations is the fact that they are typically only valid over a specific range of conditions, such as Reynolds number, length scales, etc. Even if one is a fervent believer that empirical correlations are accurate, it is still critical that one understands the conditions under which a correlation was developed, and ensures that the correlation is considered to be appropriate for the specific case in which it is being used.

While Clemens' concerns with correlations are certainly valid, I didn't always take them as seriously as I possibly should have. I felt that most the more widely accepted correlations were probably reasonably accurate and most engineers are aware enough to be sure that a given correlation is appropriate for their application. I was recently reminded that this isn't always the case when I came across a paper that dealt with from a near-nanoscale structure. The paper used a fairly widely known correlation [4] to estimate the free convection from a very small cylinder that had a diameter of a few microns. The results reported in the paper had what seemed to be quite high heat transfer rates, given that it was for a case of natural convection. Upon further review of the details of the analysis, it turned out that the conditions under which the analysis was done were below the range for which the correlation was considered to be appropriate. The very small diameter led to an extremely small Rayleigh number that was at least two orders of magnitude below the data from which the correlation was developed. This led to a heat transfer, in free convection, that was more than 5,000 W/m^2 K.

A close review of reference [4] reveals a few interesting details. First, the log-log charts that compile dimensionless data appear to have errors in the labels for the y-axis. While the correlation appears to be correct despite the errors in the plots, this is a reminder that empirical correlations should be verified to ensure that an error did not find its way into the analysis. Another issue of note in the original paper is an explicit recognition that the correlation is not valid for Rayleigh numbers (Ra) less than 10^{-6}, which is much larger than the situation calculated for a micron-scale cylinder. Using empirical correlations can always be somewhat dangerous—particularly when they are used outside the range of conditions for which they were developed.

When I first began writing this article, I was fairly certain that I was writing about an excellent example of an empirical correlation being badly misused. The micron-scale cylinder in the paper that I found had a Ra on the order of 10^{-10}, which was four orders of magnitude outside the appropriate range for the correlation. However, after spending far more time trying to interpret reference [5] than I ever intended (primarily because of the errors in the scales used in the plots), it appears that there are data for ex-

tremely small Ra values and the error in using the correlation for the micron-scale may closer to a factor of 2, rather than the orders of magnitude that I first thought.

While the concerns about correlations discussed in references [1-3] are certainly valid, I still believe that empirical correlations can be useful for generating preliminary assessments of a system, as long as their limitations are recognized, and the application is sufficiently similar to the test conditions that were used to generate the correlation. This becomes more important, and challenging, as we move into applications with world of micro- and nano-scale geometries. These tiny geometries can lead us astray by introducing errors because we are extrapolating them to conditions that are not relevant. Or, they can possibly lead us to significant heat transfer improvements (5 kW/m^2 K in free convection!) if they are still correct at those geometries and we can determine ways to exploit them.

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[1] https://www.electronics-cooling.com/2010/04/thermal-facts-and-fairy-tales-most-of-us-live-neither-in-wind-tunnels-nor-in-the-world-of-nusselt/ (accessed 8/4/19)

[2] https://www.electronics-cooling.com/2011/09/thermal-facts-and-fairytales-does-your-correlation-have-an-imposed-slope/ (accessed 8/4/19)

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Thermal Interactions Between High-Power Packages and Heat Sinks, Part 2

Reprinted from the March, 2011 issue. To be followed by a new Part 3, planned for Spring, 2020 issue.

Bruce Guenin
Associate Technical Editor

INTRODUCTION

These days, many thermal engineers face the challenge of defining effective heat sink cooling solutions for high power processors and ASICs (Application-Specific Integrated Circuits). The usual practice would be to calculate a value of $_{JA}$ (junction-to-air thermal resistance) for the combined package/heat sink assembly and compare it to the requirements of the application.

Traditionally, in performing this sort of calculation, one would first obtain a value of Θ_{JC} (junction-to-case thermal resistance) from the packaging supplier and a value of Θ_{SA} (sink-to-air thermal resistance) from the heat sink supplier. Since the heat sink test is usually performed with a uniform heat flux applied over the entire base, one would need to correct the value of Θ_{SA}, assuming that the heat is transferred into the heat sink uniformly over the entire contact area between the package and the heat sink. A very accurate and efficient method of doing this has been described in this publication [1]. One would then make assumptions about the thickness and thermal conductivity of prospective thermal interface materials (TIMs) to provide effective thermal contact between the package and the heat sink. The thermal resistance of this particular TIM, between the package case and the heat sink base (namely, TIM2) is referred to as Θ_{CS}.

The three thermal resistance values would then be added up to obtain the desired value of Θ_{JA} per the following expression:

$$\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA} \quad (1)$$

This procedure worked well enough when power levels were lower than today. The accompanying higher values of thermal resistance masked the presence of certain thermal interactions that are important sources of error for high-power/low-thermal-resistance components. The fact that these resistances are not boundary-condition independent means that their precise value depends upon the details of the heat transfer between the various components [2]. This is due to the fact that these thermal resistance metrics are the product of a methodology, which ultimately represents a measurement approach: namely the temperatures T_J, T_C, and T_S, all are determined at the geometric center of each component [3]. Such single-point temperature measurements do not provide direct information regarding the heat flux distribution that could be useful in defining a more robust thermal resistance metric.

SUMMARY OF PART 1

Part 1 of this article was devoted to exploring the nuances of the interactions between these components, particularly as to their effect on the heat flux distribution in the path between the package case and the heat sink base [4].

Figure 1 depicts a typical configuration of a flip-chip cavity package containing a copper lid in contact with the base of a heat sink. Those components depicted using bold colors are explicitly represented in the Finite Element Analysis (FEA) model. These constitute the primary heat flow path, from the chip to the heat sink. Those drawn with the faint colors are present in the physical assembly, but are not explicitly represented in the model. These include the heat sink fins and the package substrate and the printed circuit board (PCB) to which the package is electrically interconnected. The cooling effect of the fins is accounted for by the use of an effective heat transfer coefficient (h_{EFF}) applied to the top of the heat sink base. The heat flow through the package substrate to the PCB is simply ignored, since in a high-power package, it is of secondary importance.

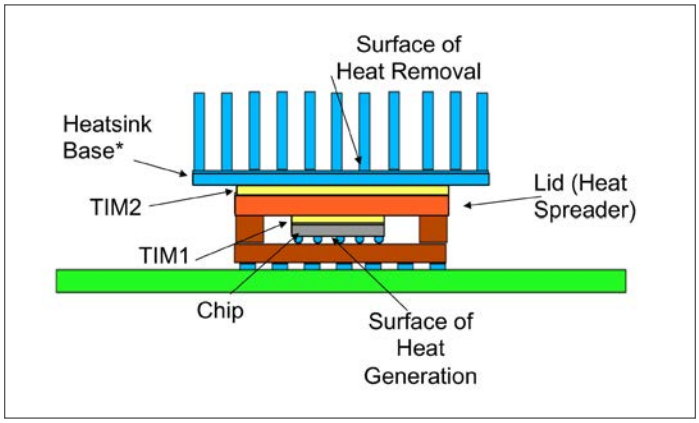

Figure 1. Diagram of high-power package attached to a heatsink. Components in bold color are explicitly represented in the model. Those in a faint color are part of the physical assembly, but are not represented in the model.

Model Dimensions, Materials, and Properties						
Layer No.	Component	Thickness	Width	Material	Th. Cond	Heat Transfer Coef.
		(mm)	(mm)		(W/mK)	(W/m^2K)
1	Die	0.5	13	Si	111	N/A
2	TIM1	0.1	40	Ag-Epoxy	2	N/A
3	Lid	0.5	40	Cu	390	N/A
4	TIM2	0.05	40	Grease	1	N/A
5	Heat Sink Base	2	40, 70, 100	Low-Cond Al Alloy	166	50, 200, 1000, 2000
		2	40, 70, 100	High-Cond Al Alloy	240	50, 200, 1000, 2000
		6	40, 70, 100	Cu	390	50, 200, 1000, 2000

Table 1. Model Dimensions, Materials, and Properties.

Table I defines the package construction and the variations in the heat sink design explored. The heat sink designs and the large spread in h_{EFF} represent a wide range of thermal performance.

The curved data sets in *Figure 2* demonstrate the heat flux distribution through the TIM2 material determined for the lowest and highest conductivity heat sinks, at a value of heat sink width, w_{HS} = 70 mm, and over the full range of h_{EFF}. They show that, even for a package with a 1 mm thick lid made of pure copper, the heat flux is concentrated in the center of the package, in stark contrast to the traditional assumption of uniform heat flow over the package area.

The rectilinear data sets represent a uniform flux distributed over a specified area defined herein as the Heat Transfer Area (HTA). The HTA was defined in Part1 as: the area bounding a uniform flux region which produces the same value of Θ_{SA} as the FEA simulation with non-uniform flux distribution, each with the same total power. This procedure was decided upon because of its simplicity, rather than pursuing the more involved process of analyzing the actual flux distributions. For a square shaped die and package, such as in the current example, it is convenient to refer to the HTA Width, which provides a more intuitive sense of the size of the area than referring to the area itself.

DERIVATION AND USE OF THE HTA CONCEPT

Figure 3 (see page 22) shows curves of Θ_{SA} versus the full range of values of HTA Width possible with the present package: from the die width (13 mm) to the full package width (40 mm). These curves were calculated using FEA with only the heat sink base in the solid model and applying the flux at HTA values equal to 13, 20, 30, and 40 mm sq. (Note that this calculation could have been performed with equal accuracy using the method in *Reference 1*.) The curves were created using a third-order linear regression technique.

The symbol overlapping each curved line represents a value of HTA which yields a value of Θ_{SA} equal to that calculated in the

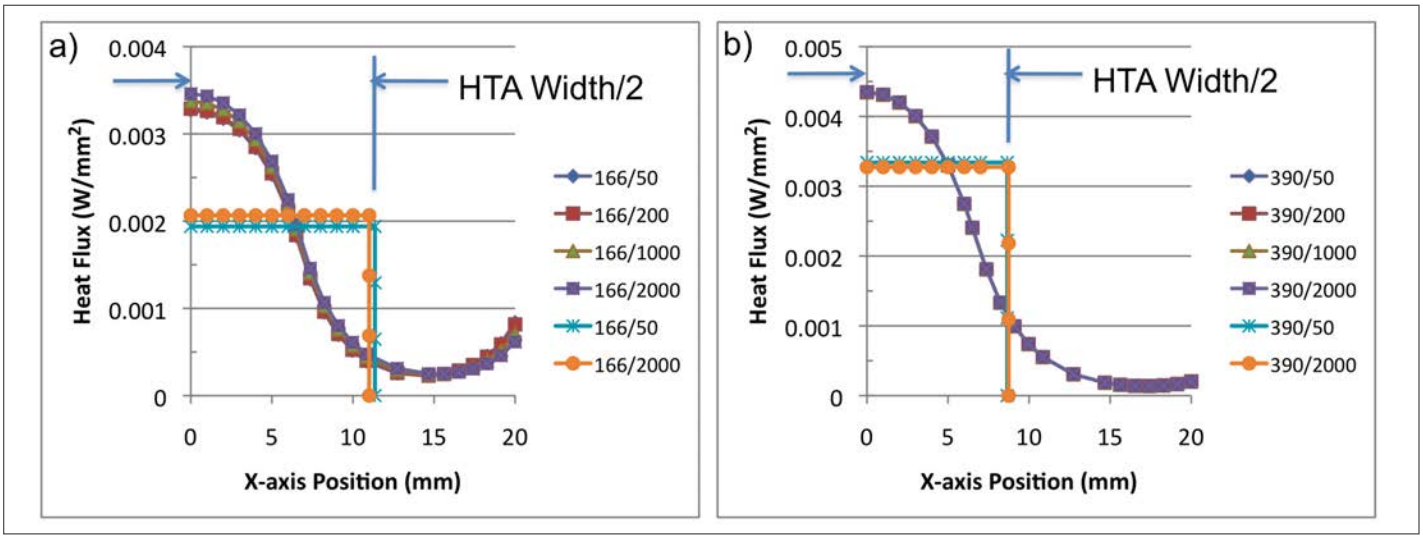

Figure 2. Plot of heat flux in TIM2 region, at specific values of k_{HS} and h_{EFF}. w_{HS} is constant at 70 mm. Curved data set: values extracted from full FEA model. Rectilinear data set: representation of HTA with constant flux. a) low conductivity Al heat sink; b) Cu heat sink.

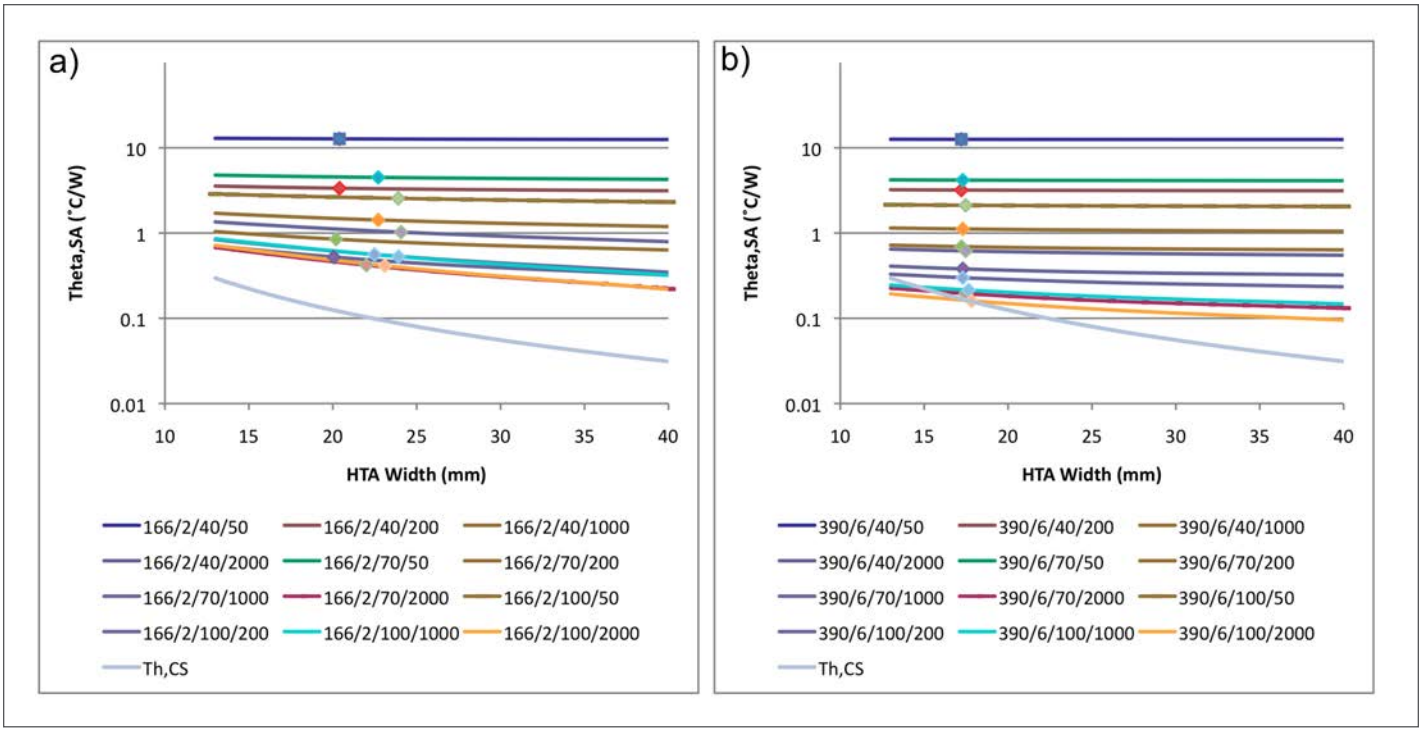

Figure 3. Plot of Θ_{SA} versus HTA Width at specific values of k_{HS}, w_{HS}, and h_{EFF}. Symbols represent FEA result for Θ_{SA} at intersection with Θ_{SA} curves, used to determine value of HTA for each heat sink condition. Lowest curve is Θ_{CS} vs HTA. a) low conductivity Al heat sink; b) Cu heat sink.

full FEA model of the package in contact with the heat sink. A spreadsheet solver was used in the calculation. For the low conductivity heat sink they are clustered in the range of HTA Widths between 20 and 24 mm. For the high conductivity heat sink they are in the narrower range between 17 and 18 mm.

It is reasonable to expect that the HTA concept should be useful in the calculation of $_{CS}$, as suggested by a comparison of the uniform flux distribution over the HTA and the actual flux distribution in *Figure 2*. Since the flux is assumed to be uniform within the HTA, the following expression, representing one-dimensional heat flow, can be used to calculate Θ_{CS}:

$$\Theta_{CS} = \frac{t_{TIM\,2}}{k_{TIM\,2} * HTA} \qquad (2)$$

Where t_{TIM2} and k_{TIM2} are the thickness and thermal conductivity of TIM2, respectively. Θ_{CS} is plotted as a function of HTA in *Figures 3a* and *3b*. It is useful to compare the magnitude of Θ_{CS} and Θ_{SA} for the two heat sinks studied. For the low conductivity heat sink, Θ_{CS} is much lower than the lowest value of Θ_{SA}. In the case of the high conductivity heat sink, Θ_{CS} is comparable in magnitude to the lowest values of Θ_{SA}. This fact will be relevant during the error analysis.

Figure 4 shows the calculated values of Θ_{JC}, plotted versus the heat sink thermal conductivity, k_{HS}, for all the cases studied. It also displays a value of Θ_{JC}, calculated under simulated JEDEC-standard conditions (water-cooled cold plate, 2-mm-thick copper top plate) [5]. Note this it is a bit lower in magnitude (0.002˚C/W) than the values of Θ_{JC} calculated for the package in contact with the copper heat sink, due to its greater thickness (6 mm vs. 2 mm). Θ_{JC} values calculated for the lowest conductivity heat sink are about 0.01˚C/W less than the simulated test value. Comparing these differences with the values of Θ_{SA} and Θ_{CS} in *Figure 3* suggest that these deviations in Θ_{JC} in the full model from the simulated test value will not be a significant source of error.

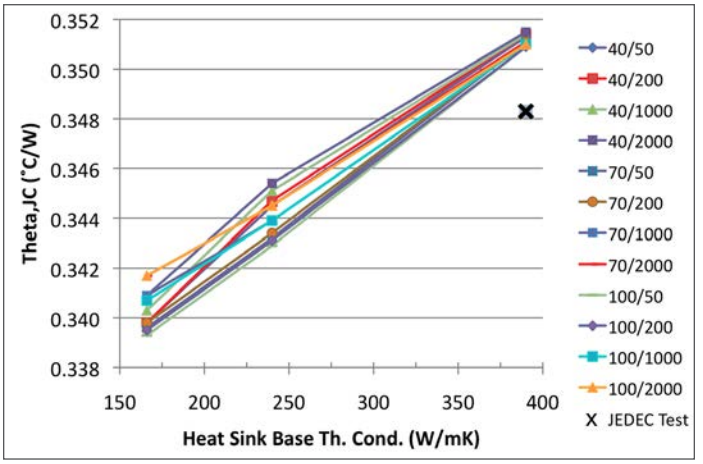

Figure 4. Plot of Θ_{JC} versus vs k_{HS} at specific values of w_{HS} and h_{EFF}: extracted from full package/heat sink FEA simulation. Black X symbol represents simulated JEDEC test result.

Figure 5 (see page 23) contains a plot of Θ_{CS} versus HTA Width. The values of $_{CS}$ were calculated using one of two methods: 1) extraction from the full package/heat sink FEA simulation and 2)

calculation using *Equation 2* and the values of HTA calculated using the method illustrated in *Figure 3*. The HTA-calculated values are approximately 0.08˚C/W less than the FEA-calculated values for the low conductivity heat sinks and 0.05˚C/W less for the high conductivity heat sinks. Comparing these discrepancies with the values of Θ_{SA} in *Figure 3*, suggest that this will be a more significant source of error.

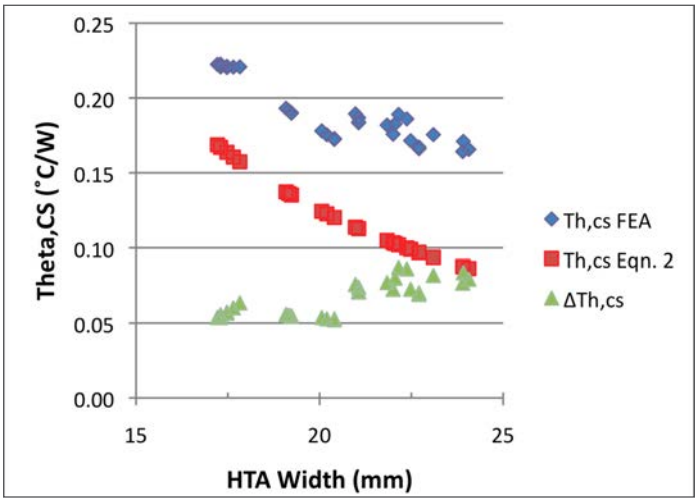

Figure 5. Plot of Θ_{CS} versus HTA. Blue symbols: values extracted from full package/heat sink FEA simulation. Red symbols: values calculated from Equation 2.

SIMPLIFIED THETA, JA CALCULATIONS USING THE HTA CONCEPT

It is hoped that the preceding analysis has made it clear that the assumed size of the area bounding the heat flow between the package and the heat sink has a significant influence on the resultant values of Θ_{CS} and Θ_{SA} and, consequently, Θ_{JA}. This section will explore the accuracy of analytic calculations making various assumptions regarding the size of this bounding area.

Analytical Model Assumptions and Error Analysis

Method #	Areas Assumed in	Error		
		Avg	Max	Min
1	Pkg	-21%	-2%	-36%
2	Avg HTA, all cases	-5%	3%	-16%
3	HTA - Avg per HS Type	-4%	-1%	-10%
4	Specific HTA value	-4%	0%	-9%

Table 2. Analytical Model Assumptions and Error Analysis.

Table 2 describes four methods, which differ in this assumption.

- Method #1 assumes the bounding area = the package area.
- Method #2 assumes the bounding area = a single value of HTA averaged over all the cases studies.
- Method #3 assumes the bounding area = average of HTA calculated for each of three heat sink configurations.
- Method #4 assumes the bounding area = the specific value of HTA calculated individually for each case.

Θ_{JA} is calculated using *Equation 3*:

$$\Theta_{JA} = \Theta_{JC,TEST} + \Theta_{CS}(Area)\,[Eqn.2] + \Theta_{SA}(Area)\,[\text{Ref. 1}] \qquad (3)$$

The results calculated using each method were compared to the Θ_{JA} values calculated using the original FEA model. A complete listing of all the Θ_{JA} results is provided in *Table 2* of Part 1 of this article [4]. The results are shown in *Figure 6*. The error is summarized in *Table 2*.

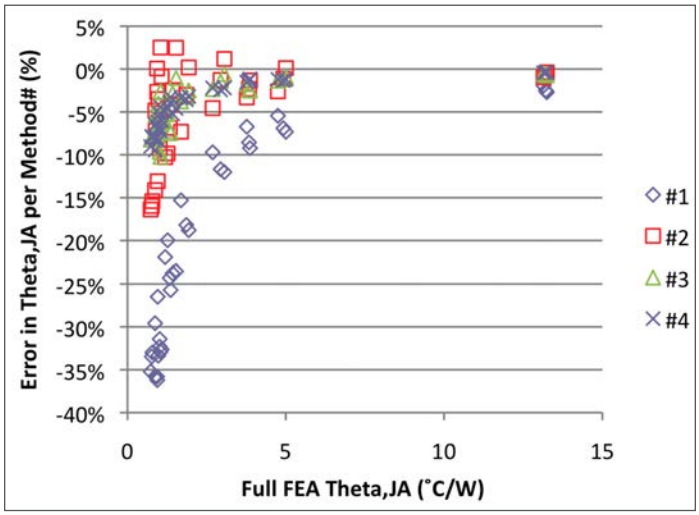

Figure 6. Error in value of Θ_{JA}, calculated using Equation. 3 versus Θ_{JA}, extracted from full package/heat sink FEA simulation. Results reflect effect of four different assumptions regarding the method of calculating the heat transfer area.

All the methods show an increase in the absolute error as the value of Θ_{JA} gets smaller. Method #1, using the package size for the heat transfer area, has an error of less than 10% for values of Θ_{JA} of 3˚C/W and greater. For Θ_{JA} values of less than this, the error grows to 36%. Using the average HTA value of 20.6 mm, in Method #2 leads to a large reduction of error, with the maximum error equal to 16%. Further improvement is obtained with Method #3, using the value of HTA averaged for each heat sink design. Here the maximum error is 10%. Method #4, with a separate value of HTA applied to each case represented a small improvement with the maximum error equal to 9%. As indicated earlier, most of the error in Methods #4 and 5 is due to the Θ_{CS} term.

CONCLUSIONS

The past practice of assuming a uniform heat flow between a package and heat sink over the full area of the package is shown to be inadequate with high-power packages. The HTA method uses the same assumption of a uniform flux as before, but uses a value for the bounding area determined from a detailed finite element analysis of the package and heat sink. For this method to become more widely useful, correlations are needed to generate appropriate HTA values for arbitrary package and heat sink designs. Once the appropriate HTA is on hand, then the remainder of the calculation is straightforward.

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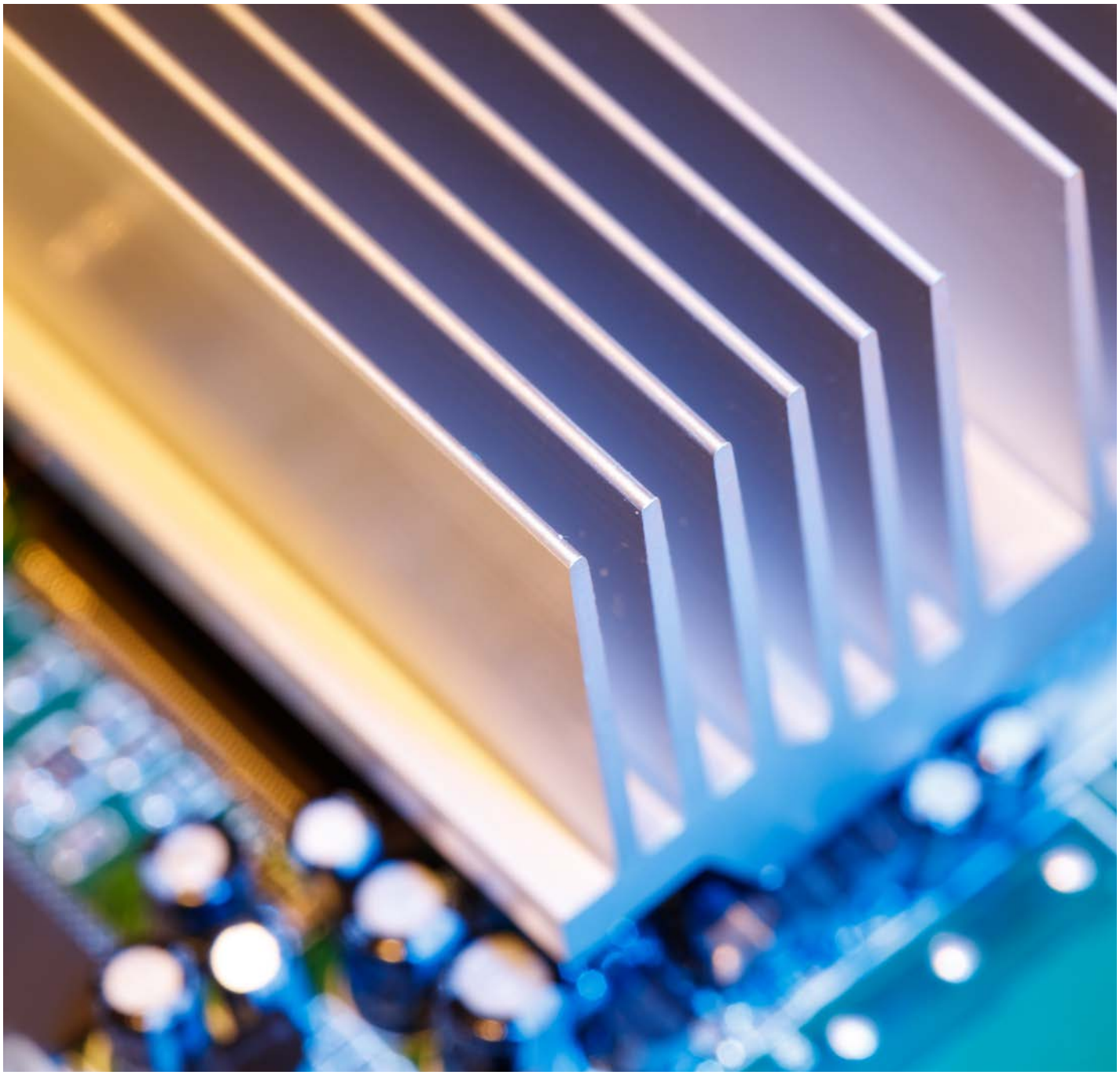

Summary of the IEEE ITherm 2019 Conference

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The IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm) was held at the Cosmopolitan Hotel and Casino in Las Vegas, NV from May 28-31, 2019. This was the 31st Anniversary of ITherm, first held in 1988. The conference was historically held every other year until 2016 when it switched to an annual schedule, making this the 18th ITherm. ITherm 2019 was sponsored by the IEEE Electronics Packaging Society (EPS) and co-located with the 69th Electronic Components and Technology Conference (ECTC 2019).

The ITherm 2019 program consisted of 18 professional development workshops on Tuesday, May 28, 2019, followed by three full days of technical presentations in four tracks with 50 sessions, in which 181 papers were presented. Additional technical events included three keynote addresses, five panels, five technology talks, a student poster competition, and an Art-in-Science competition. Of note was a presentation session by students competing in the second annual heat sink design competition, hosted by ASME/K16 and EPS. There were also two panels held jointly with ECTC–the ECTC/ITherm Young Professionals Panel and the ECTC/ITherm Joint Women's Panel, "Unleashing the Power of Diversity in the Workforce." Both panels were sponsored by EPS and provided an opportunity for closer interaction between the attendees of the two conferences.

This year saw several new additions to the conference, including an improved mobile app, a heat sink design competition, and demonstrations of air, dry ice, and liquid nitrogen cooling by the Oregon State University Overclocking team. An *ITherm LinkedIn page* was introduced in 2018, which we invite you to join to keep up with announcements and deadlines for ITherm 2020.

RICHARD CHU ITHERM AWARD FOR EXCELLENCE

Prof. John R. Thome was awarded the Richard Chu ITherm Award for Excellence for his pioneering work on multiphase flows. Dr. Thome is Professor-Emeritus of Heat and Mass Transfer at the Ecole Polytechnique Fédérale De Lausanne (EPFL), Switzerland, and founder of JJ Cooling Innovation Sàrl in Laussane. Through decades of research, his work has produced new insights into micro channel flow boiling, new flow visualization/image processing techniques, flow stabilization, heat transfer models, flow pattern maps, micro-two-phase cooling systems, and numerical modeling of bubbly/slug flows.

KEYNOTES

On the first day of the conference, Dr. Guarang Choksi, vice president of technology development and director of assembly and test technology development at Intel, gave a keynote address entitled "Component Integration vs. Product Differentiation: Electronic Packaging Choices for Heterogeneous Assembly & Test." Dr. Choksi discussed the need for interdisciplinary tools for analysis, simulations, and characterization to meet to heterogeneous packaging needs of the future as we move toward 2.5D and 3D architectures.

On the second day of the conference, Dr. Andrew Alleyne, Ralph & Catherine Fisher Professor, University of Illinois, Urbana-Champaign, gave a keynote address entitled "A Systems Approach to Management of Transient Thermal Systems for Mobile Electrification." Dr. Alleyne illustrated the use of a systems-based framework to control the complex electro-thermal interconnected subsystems on board modern transportation platforms.

On the final day of the conference, Cullen Bash, vice president and director of the Systems Architecture Lab at Hewlett Packard, gave a keynote address entitled "Computing beyond Moore's Law." This talk described the transition from traditional CPU driven computing to a memory and data driven model with specialized devices and the challenges this transition places on traditional architectural elements.

BEST AND OUTSTANDING PAPERS

An awards luncheon was held on the final day of the conference, at which awards for the best and outstanding papers in each track, based on judging from reviews and inputs from session and track chairs, were unveiled to the attendees.

Best Papers

Component Level Thermal Management

- Piyas Chowdhury, Kamal Sikka, Alfred Grill, Dishit P. Parekh, "Optimal Filler Sizes for Thermal Interface Materials," IBM.

System Level Thermal Management

- Shurong Tian, Todd Takken, Mark Shultz, Chris Marroquin, Vic Mahaney, Yuan Yao, Michael J Ellsworth Jr, Anil Yuksel, Paul Coteus, "A Single Flexible Cold Plate Cools Multiple Devices," IBM.

Mechanics and Reliability

- Rainer Dudek, Kerstin Kreyssig, Sven Rzepka, Michael Novak,

Wolfgang Gruebl, Peter Fruehauf, Andreas Weigert, "Comparisons of Solder Joints Fatigue Life Predictions and Several Long-Term Testing Results," Fraunhofer ENAS Micro Materials Center, Continental, and Siemens.

Emerging Technologies & Fundamentals

- Ziqi Yu, Zongqing Ren, Jaeho Lee, "Investigation of Thermal Metamaterials Based on Nanoporous Silicon Using Ray Tracing and Finite Element Simulations," University of California — Irvine.

Outstanding Papers

Component Level Thermal Management

- Prabhakar Subrahmanyam, Arun Krishnamoorthy, "Micro-Scale Nozzled Jet Heat Transfer Distributions and Flow Field Entrainment Effects Directly on Die," Intel.

System Level Thermal Management

- Anirudh Krishna, Jin Myung Kim, Juyoung Leem, Michael Cai Wang, SungWoo Nam Jaeho Lee, "Dynamic Radiative Thermal Management by Crumpled Graphene," University of California—Irvine and University of Illinois at Urbana Champaign.

Mechanics and Reliability

- A R Nazmus Sakib, Richard S Lai, Sandeep Shantaram, "Effects of Solder Mask Application Method on the Reliability of an Automotive Flip Chip PBGA Microcontroller," NXP Semiconductors.

Emerging Technologies & Fundamentals (Tie)

- Martinus Arie, David Hymas, Farah Singer, Amir Shooshtari, Michael Ohadi, "Performance Characterization of a Novel Cross-Media Composite Heat Exchanger for Air-to-Liquid Applications," University of Maryland.

- Aaditya Anand Candadai, Justin Weibel, Amy Marconnet, "A Measurement Technique for Thermal Conductivity Characterization of Ultra-High Molecular Weight Polyethylene Yarns Using High-Resolution Infrared Microscopy," Purdue University.

We are also pleased to announce that the ITherm 2019 Proceedings have been forwarded to the IEEE Xplore Digital Library and will be posted soon. Papers appearing in the Table of Contents are available for access and download, along with listings of our Keynote Speakers, Tech Talks, Panels, Sponsors, and Exhibitors.

ASHRAE Technical Committee 9.9: Mission Critical Facilities, Data Centers, Technology Spaces, and Electronic Equipment

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NOMENCLATURE

A1, A2, A3, A4	ASHRAE allowable thermal envelopes as defined in *Thermal Guidelines for Data Processing* Environments that represent where IT manufacturers test equipment to ensure functionality
ASHRAE	American Society of Heating, Refrigerating and Air-Conditioning Engineers
CAGR	Compound Annual Growth Rate
*CITE*A	SHRAE Compliance for IT Equipment
Datacom	Data processing and communication facilities, that include rooms or closets used for communication, computers, or electronic equipment
DCIM	Data Center Infrastructure Management
ELC	Electrical Loss Component per ANSI / ASHRAE Standard 90.4 – 2016. The design ELC is the combined losses of three segments of the electrical chain: incoming electrical service segment, UPS segment, and ITE distribution segment.
ESD	Electro-static discharge
HVAC	Heating, ventilation and air conditioning
IT	Information Technology
MLC	Mechanical load component per ANSI / ASHRAE Standard 90.4 – 2016 is calculated by the sum of all cooling, fan, pump, and heat rejection annual energy use divided by the data center ITE energy (annualized MLC) or the sum of all cooling, fan, pump, and heat rejection design power divided by the data center ITE design power (design MLC).
TC	Technical Committee
W1 – W5	ASHRAE liquid cooling classes for liquid-cooled IT equipment

HISTORY OF ASHRAE TC 9.9

In 1999, a group of thermal engineers from different IT manufacturing companies formed a thermal management consortium. This consortium evolved into ASHRAE Technical Committee 9.9 (TC 9.9). This history was documented in articles by Roger Schmidt (2012) [1] and Don Beaty (2005) [2]. This article serves as a continuation of those articles in documenting the activities of TC 9.9 since then.

TC 9.9 was formed in response to the lack of effective information transfer between the building, HVAC, and IT industries. Its mission is to be recognized by all areas of the datacom industry as the unbiased engineering leader in HVAC and an effective provider of technical datacom information. Since its formation, TC 9.9 has grown to be one of the most active ASHRAE technical committees, and its largest, with roughly 400 members. The committee is represented by a wide range of disciplines within the datacom industry, including, producers of datacom equipment (i.e. computing hardware, software, and services), producers of facility equipment (i.e. HVAC, DCIM, rack, and power solutions), users of datacom equipment (i.e. facility owners, operators, and managers), and general interest (i.e. government, utilities, consultants, academia, and laboratories).

Dustin Demetriou
Dr. Dustin Demetriou is a Senior Engineer at IBM Corporation in the IBM Systems' Advanced Thermal Energy Efficiency Lab. He received a Ph.D. in Mechanical and Aerospace Engineering from Syracuse University. His research is focused on the analysis, application, and optimization of energy conversion systems, particularly in the area of high-density data centers and high-performance buildings, and the development of advanced electronics cooling technologies. He is the Chair of ASHRAE Technical Committee 9.9 on Mission Critical Facilities, Data Centers, Technology Spaces, and Electronic Equipment.

The activities of TC 9.9 have spanned all aspects of data center design and operation. *Figure 1* provides a historical perspective on the activities of the committee, dating back to its formation in 2004. One of the cornerstone contributions of TC 9.9 has been the Datacom Series books. The series started with the publication of the *Thermal Guidelines for Data Processing Environments* and has been expanded to include a diverse range of topics, including data center structural and vibration guidelines, server performance characterization, and particulate and gaseous contamination, to name a few. As of the publication of this article, 14 books have been released with several having multiple editions. These books serve as essential training for anybody with an interest in the datacom industry and have become global resources, with several having been translated into Mandarin and Spanish, and others being incorporated into regulation to support data center energy efficiency initiatives. In addition to the book series, TC 9.9 has played a role in the development of other significant resources. Historically, TC 9.9 has initiated a new topic through the publication of a white paper, which is made freely available to the industry. This allows the material to be published in a timely fashion as either demand is expressed by the industry or a significant gap is seen in the industry by the committee. Subsequently, in many cases, this material is further developed and expanded into a Datacom Series book. To supplement these activities, TC 9.9 also engages in industry/academia research programs. Furthermore, the material in these publications is used to develop other resource available through ASHRAE, including a new chapter in the *ASHRAE HVAC Applications* Handbook [3] and *ANSI/ASHRAE Standard 90.4-2016 Energy Standard for Data Centers* [4].

The remaining sections of this paper will highlight a few of the most recent activities of the committee that currently have broad interest amongst data center professionals globally.

THERMAL GUIDELINES FOR DATA PROCESSING ENVIRONMENTS

Now in its fourth edition, *Thermal Guidelines for Data Processing Environments* [5], remains the foundation of the Datacom series. When first established, the thermal guidelines represented the first comprehensive set of temperature and humidity conditions, established by the IT manufacturers, that linked the design of datacom equipment (i.e. servers and storage) and the data center. They established guidance to data centers on operating the datacom equipment for optimal performance, highest reliability, and lowest power consumption. This publication has become the de-facto standard for the environmental design and operation of electronic equipment installed in a datacom facility. Furthermore, in 2018, the European Commission approved an Ecodesign Regulation for servers and data storage products [6]. As part of this regulation, IT manufacturers will be required to declare the

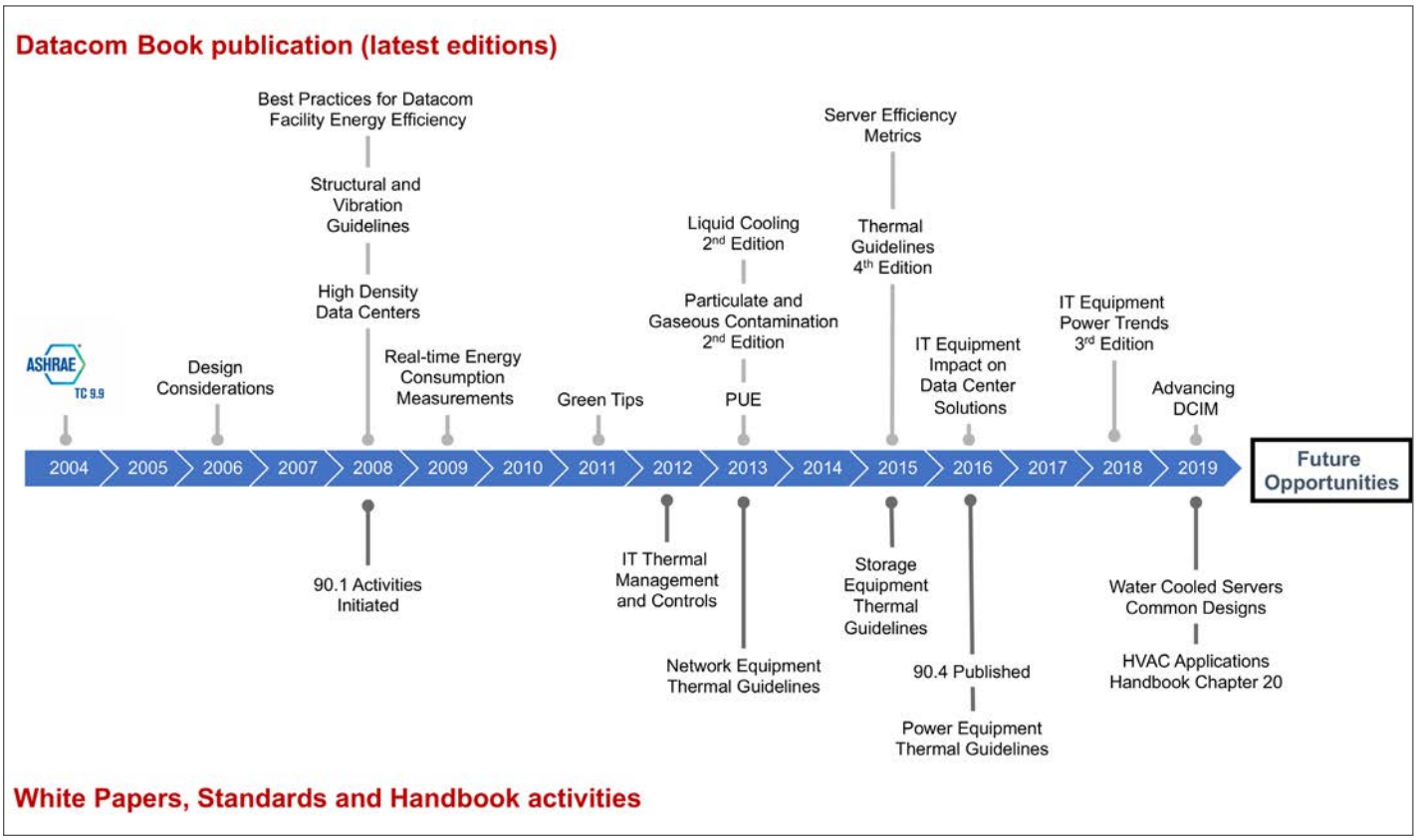

Figure 1. Timeline of ASHRAE TC 9.9 activities, including the publication of Datacom Series book, white papers, Standards, and handbook activities since its formation in 2004.

environmental class of their product according to the ASHRAE environmental classes defined in the *Thermal Guidelines for Data Processing Environments* publication.

Prior to publication in 2004 of the first edition, there was no single source in the data center industry for ITE temperature and humidity requirements. In the second edition of the *Thermal Guidelines for Data Processing Environments* the recommended envelope was expanded to provide data center operators guidance on maintaining high reliability and also operating their data centers in the most energy efficient manner. This envelope was created for general use across all types of businesses and conditions. The second edition also introduced new allowable envelopes (A1 and A2), that expanded the maximum allowable dry-bulb temperature to 32°C and 35°C, respectively, with a maximum relative humidity limit of 80% and a minimum relative humidity limit of 20%. These envelopes also differed in the maximum allowable dew point temperature. These allowable envelopes offered data center operators the flexibility in using an operating envelope that matched their business need and to weigh the balance between the additional energy savings of the cooling system versus the deleterious effects that may be created on total cost of ownership by operating outside the recommended range. With the further pursuit of energy efficiency, the third edition added two expanded allowable envelopes (A3 and A4) to the already documented A1 and A2 in the second edition. These new classes enabled near full-time use of free cooling techniques in the vast majority of the world's climates. However, using these envelopes added some complexity and trade-offs in terms of energy, reliability, and resiliency that requires more careful evaluation by the data center owner due to the potential impact on the IT equipment to be supported. The third edition also introduced, for the first time, environmental classes for liquid cooled IT equipment (W1—W5).

As the datacom industry looked to further improve data center energy efficiency, from 2011 to 2014, ASHRAE funded research [7] to investigate the risk of electrostatic discharge (ESD) related events in data centers that operate at lower humidity. The results from this study showed that data centers could be operated with relative humidity levels as low as 8% without any noticeable impact on equipment reliability. For data centers that implement a standard set of ESD-mitigation procedures, and as a result of this study, the ASHRAE environmental classes were further expanded to increase the energy saved in data centers by not requiring

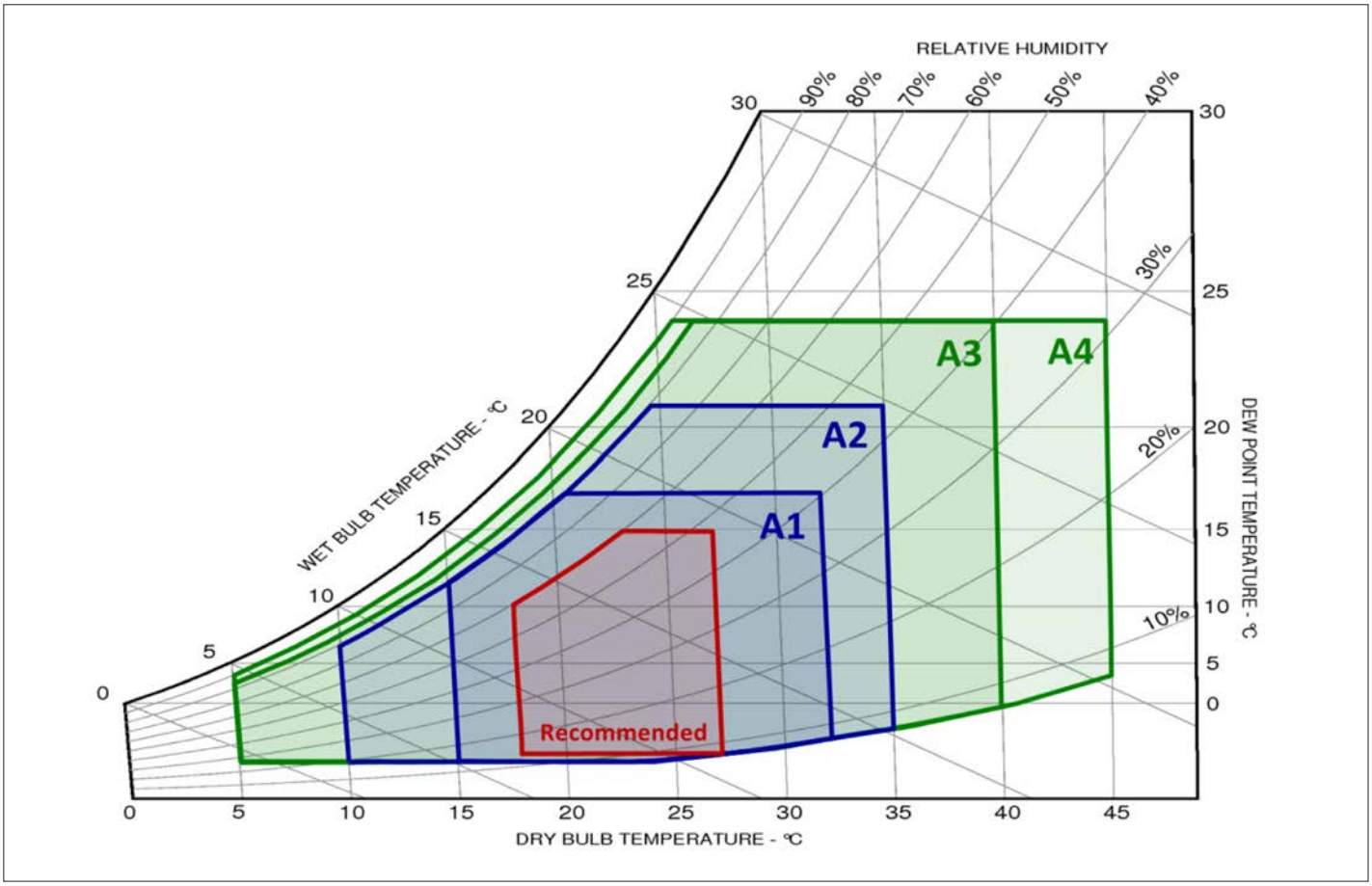

Figure 2. ASHRAE Thermal Guidelines for Datacom Equipment fourth edition psychrometric chart in SI units at sea level. These conditions pertain to the air entering the IT equipment. Refer to [5] for additional footnotes, including altitude de-rating and ESD control requirements, before using. (image courtesy of ASHRAE, originally published in [5]).

humidification at low moisture levels. These expanded envelopes are shown in *Figure 2* (see page 29). As has been the case since the second edition, the recommended environmental envelope provides guidance on where facilities should be designed to provide long-term reliability and energy efficiency of the IT equipment. The allowable envelopes (A1—A4) are where IT manufacturers test their equipment in order to verify that it will function but ultimately are meant for short-term operation. The allowable classes may enable facilities in many geographical locations to operate year-round without the use of mechanical refrigeration, which can provide significant savings in capital and operating expenses in the form of energy use.

IT EQUIPMENT POWER TRENDS

One of the first tasks of the thermal management consortium, referenced above, was the publication of power trends for IT Equipment through the Uptime Institute. About every five years, ASHRAE TC 9.9 has released updated power trends. Now in its third edition, *IT Equipment Power Trends* [8] (formerly, *Datacom Equipment Power Trends and Cooling Applications*), contains the best-known hardware power trends through 2025. For the first time in the series, the power trends have been segregated by workload type. This is a significant change from previous editions that focused only on the power trends for servers of a given form-factor (i.e. 1U vs. 2U). By delineating the power trends by workload type, it provides the user with a more customized methodology to assess the power for a given configuration and/or workload. Of most practical use in the third edition was the inclusion of the compound annual growth rate (CAGR) of power for each workload and server form-factor. Ultimately, data center owners can use the CAGR with measurements of their current system power to get realistic projections of future power needs based on their specific deployment.

The third edition of *IT Equipment Power* Trends breaks down the workload types into eight general categories: Scientific, Analytics, Business Processing, Cloud / Internet Portal Data Center, Visualization & Audio, Communications / Telco, Storage, and Networking. The power trends by workload type reflects the change in the IT industry to support users' needs in terms of server configurations, with targeted types of workloads to maximize IT equipment performance and efficiency. The impact the workload has on the overall power trends is evident from *Figure 3,* which provides a historical perspective of the power trends for 2U, 2-processor servers. It is clear that a similar server, configured differently to meet a specific workload, can have widely different power dissipation. Ultimately, the move to a workload-based power trends should go a long way in helping data center operators design a more efficient data center that supports many generations of IT equipment.

ADVANCING DCIM WITH IT EQUIPMENT INTEGRATION

The newest book in the ASHRAE Datacom Series, *Advancing*

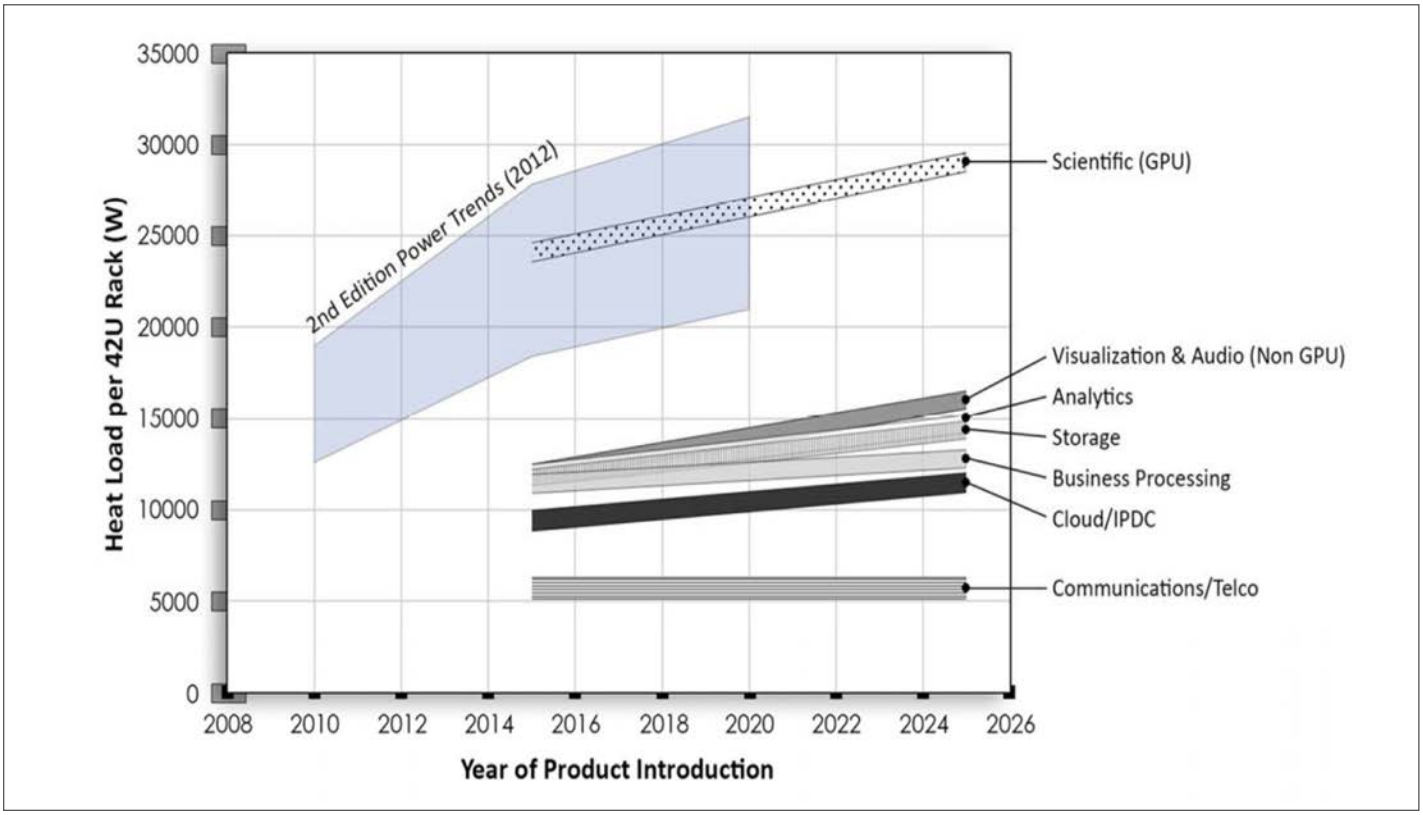

Figure 3. Evolution of the ASHRAE Power Trends from the 2nd Edition to the 3rd Edition for 2U, 2-Socket Servers (image courtesy of ASHRAE, originally published in [8]).

DCIM with IT Equipment Integration [9] aims to demystify and extend the implementation of data center infrastructure management (DCIM) tools. With the large number of available data sources within the data center, DCIM has the potential to be the next step in further improving data center energy efficiency and increasing data center resiliency. To enable a more holistic view of the data center, DCIM requires the integration of many disparate data sources—facility equipment, IT equipment, Internet of Things devices, etc. This level of integration has failed to garner wide-spread adoption due to the sheer effort required to program and implement the large number of proprietary protocols, nomenclatures and implementations on the market. ASHRAE DCIM Compliance for IT Equipment (CITE), for the first time, establishes an alignment on a common set of power and cooling telemetry and metrics within the IT industry for servers. ASHRAE TC 9.9 engaged with the industry standards body the Distributed Management Task Force (DMTF) to promote industry adoption of CITE. The DMTF Redfish implementation of CITE provides the proper schema mapping, physical context, and reading properties and has been adopted and accepted into the DMTF Redfish API Schema, release 2018.3.

Advancing DCIM with IT Equipment Integration [9] provides many more details on how an organization can leverage DCIM systems to help normalize and organize the large quantity of data that can be collected and how this data can be used to calculate key metrics to improve the data center's operation. It also highlights key use cases that are already being practiced in many DCIM deployments.

ANSI/ASHRAE STANDARD 90.4-2016 ENERGY STANDARD FOR DATA CENTER

In 2010, in an effort to promote data center energy efficiency, *Standard 90.1 Energy Standard for Buildings Except Low-Rise Residential Buildings* [10] incorporated data centers. Prior to this, data centers were exempt due to their mission critical nature. However, data centers have markedly different load profiles and rate of technology innovation compared to the general commercial building industry, making the prescriptive nature of 90.1 relatively unattractive to the data center industry. An ASHRAE Standard 90.4 committee was formed, with participation from ASHRAE TC 9.9. In 2016, *ANSI/ASHRAE Standard 90.4-2016 Energy Standard for Data Centers* [4], was released. This standard establishes the minimum energy efficiency requirements of data centers for design and construction, guidelines for creating a plan for operation and maintenance, and recommendations for utilizing on-site or off-site renewable energy resources. Standard 90.4 is a performance-based approach that provides flexibility for data center designers to innovate in the design, construction, and operations of their facility.

Standard 90.4 introduced two new design metrics: the mechanical load component (MLC) and the electrical loss component (ELC). Calculations of the MLC and ELC are made and then compared to the maximum allowable values provided in the standard. The MLC can be calculated on either an annualized or design basis and must be evaluated based on the data center's climate zone. The design ELC is the combined losses of three segments of the electrical chain: incoming electrical service segment, UPS segment, and ITE distribution segment. The designer can show compliance with Standard 90.4 by showing that either their calculated MLC and ELC values do not exceed the values contained in the standard at both 100% and 50% of the design IT load or they can follow an alternative compliance path that provides the designer a methodology to allow trade-offs between the MLC and ELC. Standard 90.4 does not use the Power Usage Effectiveness (PUE) defined by The Green Grid. One reason for this is that the PUE is an operational metric based on measured energy use data rather than design calculations. It should be recognized that the design calculations contained in Standard 90.4 would not likely match the actual operational PUE of the data center.

CONCLUSIONS

ASHRAE Technical Committee 9.9: Mission Critical Facilities, Data Centers, Technology Spaces, and Electronic Equipment remains one the most active technical committees within ASHRAE and the data center industry. The committee is currently focused on a number of efforts, including:

- Research into the impact of high humidity and gaseous contamination on IT equipment reliability.
- Guidelines for energy modeling to show compliance to Standard 90.4.
- Research on developing guidelines for computational fluid dynamics modeling of data centers.
- Creation of expanded content to support the rapidly materializing liquid cooling.

This article was certainly not inclusive of all activities undertaken by the committee. The interested reader is referred to the TC 9.9 website (http://tc0909.ashraetcs.org) for the latest information. The website contains information on TC 9.9 upcoming meetings, previous meeting minutes, whitepapers, and links to purchase the Datacom books.

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JEDEC Thermal Standards: Developing a Common Understanding

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The Joint Electron Device Engineering Council (JEDEC) was established to provide recognized technical standards for a wide range of applications, from how to handle electronic packages and defining package outline drawings, to the methods used to characterize performance, including thermal. The JC-15 committee focuses on writing thermal standards to create a common reference point for generating thermal characterization data. These standards were created with the objectives that they would be meaningful, consistent, and scientifically sound. The primary purpose for adopting and following a standard is to impose a common set of testing conditions so that equivalent results will be measured when the same packages are tested by different labs. This allows end users to compare package performance from different suppliers without concern that improved performance was attributed to more favorable testing conditions. A second application for thermal standards, although often applied incorrectly, is to calculate the junction temperature for a different environment using characterization data measured under JEDEC conditions. Unfortunately, these types of calculations often lead to erroneous estimates if thermal standards are applied incorrectly.

JEDEC thermal standards continue to evolve as more complex packages and test methods are introduced. The body of work developed to date by the JC-15 committee may be organized into three distinct groups. First, standards were written to characterize thermal resistance for single die and multi-die packages. Second, thermal standards were written specifically for LEDs, accounting for the optical component of power transmission. Third, standards were written to document methods for creating simplified thermal network models that represent boundary condition independent models for electronic packages in a user-defined environment. A historical review of early JC-15 standards is documented in an earlier article [1]. More recent additions to the JC-15 standards are provided in the following sections.

1. Traditional Thermal Resistance Measurements

JC-15 thermal standards provide guidance on the steps required to perform thermal characterization tests and how to report data including chip design, board design, and testing methods. An overview of thermal standards can be found in JESD15-12. Included are definitions for thermal resistance, methods for conducting tests, and suggestions for reporting data.

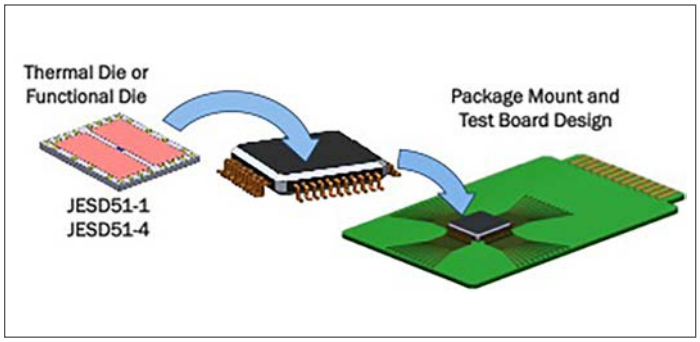

Figure 1. Preparing a package for thermal resistance measurements.

Standards were developed by documenting the steps necessary for preparing experimental test samples. These include test die and test board design as shown in *Figure 1*. JESD51-4 describes the requirements for implementing thermal die (either in wire bond or flip chip format) into a thermal test package.

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The thermal resistance is a comparative metric used to define the thermal performance of a package for a given testing environment. It is defined as the maximum die temperature, T_{Ref}, increase above the local reference temperature, T_{Ref}, per unit of power applied, see *Equation 1*. A lower resistance package will respond with a lower temperature difference compared to a higher resistance package for the same power input.

$$R_{\Theta J,Ref} = \frac{T_{j,max} - T_{Ref}}{P} \quad (1)$$

Note that the T_{Ref} is the cooling reference condition. It could be the ambient air, T_A, the package case surface, T_C, cooled by an external heat sink, or the board temperature, T_B, when cooled by a heat sink mounted to the perimeter of the test board.

Thus *Equation 1* represent three different thermal resistances; $R_{\Theta JA}$, $R_{\Theta JB}$, or $R_{\Theta JC}$, depending on the cooling environment. Heat is removed from the package by conduction when the package makes direct contact with a heat sink, $T_{Ref} = T_C$ or $T_{Ref} = T_B$, or indirectly by convection and radiation, $T_{Ref} = T_A$.

Depending on the style of the device under test, DUT, various test board designs are required to make electrical connections, either lead frame or ball array style. Several JEDEC standards were written to document test board designs for different testing conditions as shown in *Figure 2*. JEDEC test boards are relatively large, at least 76 mm x 114 mm and have thick copper on the top trace layer, at least 50 µm. They are sized accordingly to reduce the variability in thermal resistance measurements caused by variations in board fabrication, e.g. trace thickness variation.

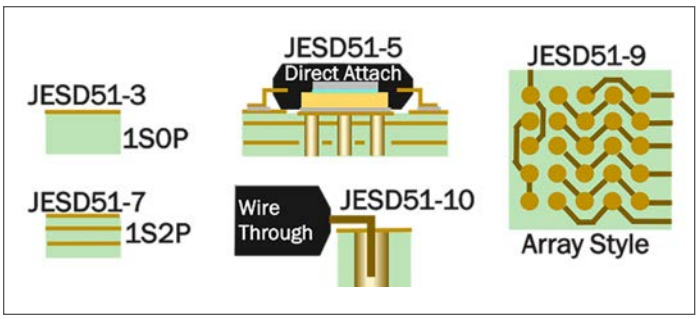

Figure 2. Board style.

An upper bound estimate on thermal resistance is made by testing packages on boards having only top layer signal traces without any internal planes (1S0P). Board design details are specified in JESD51-3. This is appropriate for applications where the test board does not have extensive power and/or ground planes, and the primary conduction path away from the package is through the traces on the top layer. When power and ground planes are included in the board, single layer traces on top layer with two internal planes (1S2P), the additional copper planes provide a conductive path to remove heat from the package. Test board design details for 1S2P are found in JESD51-7. In general, a 1S2P board will produce a junction-to-ambient thermal resistance, $R_{\Theta JA}$ that is approximately 50% less than that measured using a 1S0P board. When thermal vias are added to the 1S2P boards, making a direct path from the package to the ground plane, the thermal resistance is reduced even further. A description of the via pattern and sizes for the thermally enhanced test board design can be found in JESD51-5.

JESD51-10 provides direction for designing test boards for wire-through leaded packages. Lastly, for array style packages, including ball grid array, BGA, style packages, JESD51-9 provides guidance on test board trace fan out designs.

The environmental test conditions are described in separate standards for each type of thermal resistance. These include conduction-based tests to measure the junction-to-board resistance, $R_{\Theta JB}$, and the junction-to-case resistance, $R_{\Theta JC}$, as shown in *Figure 3*. JESD51-8 defines the conditions necessary for measuring $R_{\Theta JB}$ including the design of a double ring cold plate.

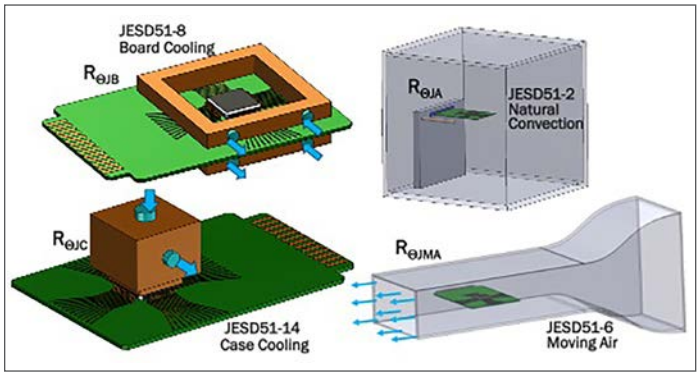

Figure 3. JEDEC-standard environments for running thermal resistance tests.

Developing a reliable method for measuring $R_{\Theta JC}$ has been a challenge due to the difficulties in accurately measuring the case temperature without influencing the heat flow path and providing a cold plate design that does not greatly impact $R_{\Theta JC}$ measurements. A steady-state $R_{\Theta JC}$ standard has been in the development stage for some time. However, limited progress has been made due to the complexities of measuring the case temperature without affecting the conductive heat flow path [2].

JESD51-14 provides a clever way for extracting $R_{\Theta JC}$ without requiring the measurement of the case temperature. It does so by making high-speed transient temperature measurements (e.g. 1 MHz) in order to capture early temperatures just as the power is turned off. At very small values of elapsed time after the power is turned off, the thermal wave has not exited the package case, and is therefore insensitive to cold plate design effects. By making two measurements, one with good thermal contact with the heat sink and a second with a thin insulator between the package and the cold plate, one can compare the two curves to arrive at an estimate for $R_{\Theta JC}$. This method should only be applied when there is one heat flow direction, e.g. die is mounted to a copper heat spreader, and should not be used if there is significant lateral heat spreading in the package.

The other two resistance, $R_{\Theta JA}$ for natural convection and $R_{\Theta JMA}$ for moving air, is shown in Figure 3. An upper bound resistance is determined for natural convection cooling using JESD51-2. The test board is inserted inside a 0.3 m x 0.3 m x 0.3 m. Weak buoyancy induced flow, caused by the heated test board and package, create a controlled natural convection boundary condition that is insensitive to external disturbance in the testing lab. For wind-tunnel testing with forced convection flow, lower resistances, $R_{\Theta JMA}$, are observed. A summary of conditions for testing DUTs under forced convection flow is found in JESD51-6.

Parameters, Ψ_{JT} and Ψ_{JB} introduced in *Equations 2* and *3* represent the junction temperature rise compared to a local referenced temperature either measured on the top of the package, T_T, or on the board, T_B, at a location 1 mm from the edge of the package. Ψ_{JT} and Ψ_{JB} measurements made during JEDEC natural convection and moving air tests, JESD51-2A and JESD51-6, can be used to estimate the junction temperature with reasonably accuracy for packages mounted in a non-JEDEC environment, e.g. on functional boards.

$$\Psi_{J,T} = \frac{T_{j,max} - T_T}{P} \quad (2)$$

$$\Psi_{J,B} = \frac{T_{j,max} - T_B}{P} \quad (3)$$

By mounting a thermocouple on top of the package and measuring T_T in the actual application, one can estimate the junction temperature as $T_{j,max} = \Psi_{JT} * P + T_T$. Similarly, if a thermocouple is mounted 1 mm from the edge of the package, one can estimate the junction temperature as $T_{j,max} = \Psi_{JB} * P + T_B$. Package vendors typically supply data for both Ψ_{JT} and Ψ_{JB} as a function of local air velocity.

The earlier package thermal test standards were developed for a single die. Hence data reporting was rather straightforward. Extension of single die package standards were made in JESD51-31 to include methods for reporting data for multi-die packages. In addition, suggestions were provided on methods for sensing the case temperature at multiple locations. The board design as outlined in previous standards became limited by the smaller number of edge connector leads available as more traces were required to support multi-die packages. JESD51-32 provides an extension to board design when the trace number becomes limited by the previously constrained connector design.

2. LED Thermal Standards

Thermal standards have evolved as new electronic package styles have been developed. For example, just 15 years ago, light emitting diodes (LEDs) where not commonly used for room illumination in residential and commercial applications. As new products are introduced, thermal standards must adapt to accommodate the latest advances in technology.

The characterization of LEDs are more challenging than electrical only packages because of the additional energy component due to light. A new series of thermal standards were written to describe conditions necessary for performing electro-optical measurements of LED packages. JESD51-50 provides an introduction to LED measurements including a description of the method to subtract the optical power from the electrical power to determine the dissipated thermal power. Details for measuring thermal resistance of LEDs are discussed in JESD51-51. JESD51-52 describes methods for measuring the optical power using an integrating sphere. More parameters are required to define the thermal resistance of LEDs than traditional packages. A summary of thermal characterization terms for LEDs are compiled in JESD51-53 and can be used as a convenient reference guide.

3. Simulation Based JEDEC Standards

It is tempting for many users to apply JC-15 thermal resistances, as supplied by package vendors, directly to predict the junction temperature while operating in a totally different system environment. Although this may be convenient since the data is readily available, the predictions cannot be expected to be accurate for different environmental conditions or for different test board design. An alternative method was needed to allow users to predict junction temperature in environments different than the standard JEDEC thermal environment. Compact thermal models were introduced as an approximation modeling method to predict junction temperature in a non-standard JEDEC environment. A compact thermal model is a simplified resistor network that approximates the three-dimensional heat conduction problem [3]. Typical electronic package models are complex having 100,000 or more nodes to represent the heat conduction analysis. Finite element analysis (FEA) methods are commonly used to solve the conduction analysis in a package. The most simplified compact thermal model available is based on a two-resistor network as shown in *Figure 4(a)* (see page 36). It has three nodes; the junction, board, and case. The top and bottom areas used to define the package are the same size as the actual package. JESD15-3 provides a description of the two-resistor thermal model.

Although the two-resistor model is quite simple, it can produce errors as great as 30% depending on the environmental conditions present in the actual system. By adding more external areas, nodes and resistors, the accuracy improves dramatically. A DELPHI [4] compact thermal model, CTM, has inner and outer areas on the top and bottom surfaces, JESD15-4. More resistors can be added to accommodate the non-isothermal areas present in the actual package. Quite often two more resistors are added to CTMs between nodes T_J and T_{BO} and between T_J and T_{TO}. Numerical values for resistors are adjusted so that the network model agrees with the detailed model over a wide range of boundary conditions applied to the external areas. Theoretically, it is possible to add even more nodes and resistors to the point where the model exactly represents the temperature field in the FEA model. Realistically, as more nodes are added to the model, the effort required to generate resistance values becomes exponentially

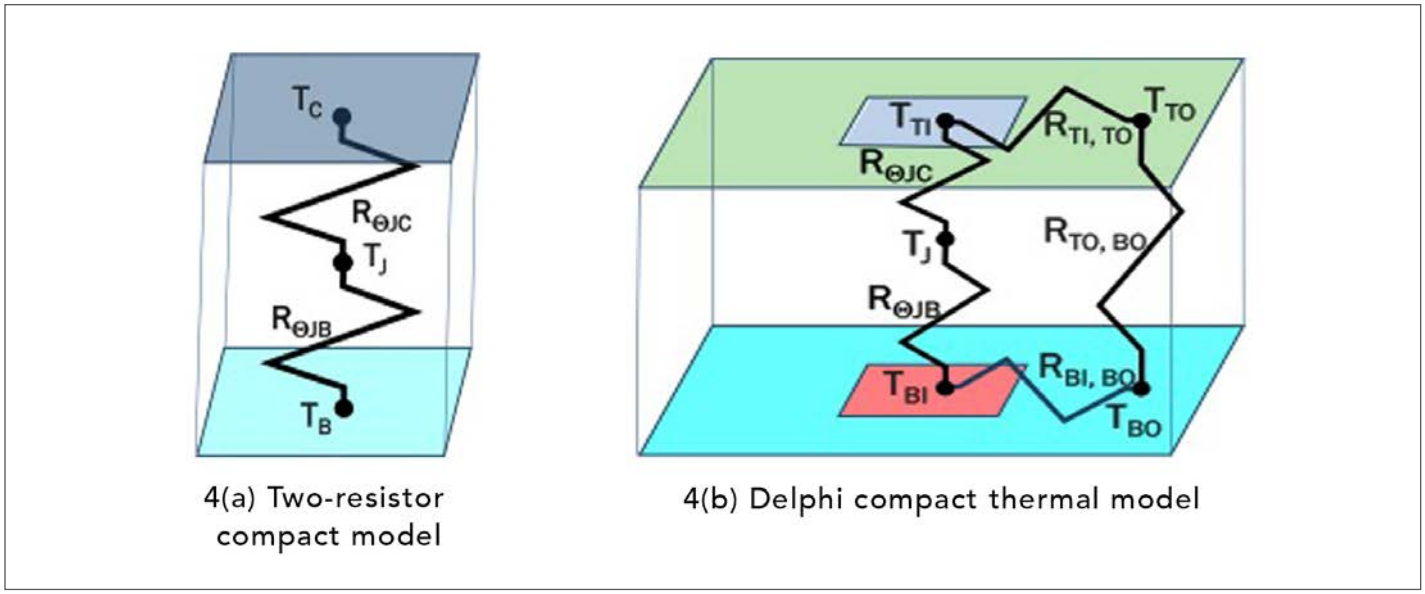

Figure 4(a) and 4(b).

more difficult. A CTM typically agrees with a detailed model for a customer environment with a difference less than 1%. These models are said to be boundary condition independent (BCI). Users can apply CTMs with confidence that they will accurately predict junction temperatures in a custom user environment. JESD15-4 provides a standard for implementing DELPHI CTMs. Notice that the standard is written for predicting steady-state conditions. CTMs can be extended to predict transient conditions by adding "thermal" capacitors between individual nodes the ambient node, see for example [5].

A more efficient means is necessary to transmit resistances, areas, and nodal topology from the package vendor to the end-user. A simple data sheet with printed numerical values is too cumbersome for exchanging model data for CTMs. A more efficient method was created using an electronic data sheet written in an eXtensible Markup Language (XML). JEDEC standard JEP 30-A100 and JEP 30-T100 provide a summary of the format used to document CTM models. A definition file, called a schema, is available on the JEDEC website that will provide a starting point for documenting CTMs.

With the introduction of two-resistor and CTMs, the end user can create accurate system level thermal models for steady-state and transient conditions with one caveat. It is best used for package with a single die. There are methods for creating CTMs for multi-die packages but the optimization problem becomes extremely difficult and cannot in general be applied reliably for all types of packages and conditions. The prevailing trend in package design is to include more heat dissipating die into individual packages called multi-chip modules, MCMs.

To overcome this difficulty, a totally different approach was taken by the package simulation software vendors. Rather than rely on a resistor/capacitor network with a physical structure, a reduced order model, ROM, was developed. A good overview of ROMs can be found in [6] and [7]. Currently there are no JEDEC standards for ROMs. However, due to the popularity and availability of simulation software to generate ROMs, new standards will be required to provide a common framework for exchanging data between package suppliers and system designers.

The JC-15 thermal committee continues to support new thermal standards that respond to changes in package styles and methods for generating thermal models. All JEDEC standards referenced here can be downloaded free of charge by accessing the given URL [8] with the specific standards number of interest. Meetings are held three times a year and are open to JEDEC members and the general public. A meeting schedule for JC-15 can be found on the JEDEC website, www.jedec.org.

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Heat Spreader Efficiency Improvements by Addition of Latent Heat Solution Materials

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INTRODUCTION

Electronics thermal management has become an increasingly important design focus as devices have become more constrained, more powerful, more expensive and more ubiquitous. To manage temperatures, particularly in mobile devices, thermal engineers typically use higher thermal conductivity components and materials. Electrical engineers strive to spatially distribute the higher power components, and also to throttle workloads to manage the peak temperatures. Latent heat storage materials (LHS materials), sometimes referred to as phase change materials (PCMs), can be useful in reducing the temperature peaks during periods of high compute and communication workloads, and thus, reduces the demands placed on the thermal conduction and power throttling capabilities of the device.

Since PCMs typically have a low thermal conductivity, they are normally integrated with a second, higher-thermal-conductivity material to optimize their performance in an application. This is usually accomplished by mixing higher conductivity particles in a matrix consisting of the PCM. However, the low value of the effective thermal conductivity of the resultant composite material, ~1 W/m-K, requires that all the PCM material be located directly in the heat flow path from the heated component to the heat sink. In order to get sufficient mass of PCM to absorb the required amount of heat during the power transients, it is normally necessary to have a thickness of several millimeters [1]. Thicknesses of this magnitude have been successfully integrated into larger mobile devices, such as tablets. However, they are too thick to be integrated into the thin-form-factor smartphones of today.

By applying the PCMs as a solid coating on a high-thermal-conductivity substrate (k > 150 W/m-K) the PCM can extend beyond the heat flow path and achieve the required volume of PCM, but at a smaller thickness than with a more conventional PCM. High-thermal-conductivity materials such as copper, graphite, and AlN have been successfully used as substrates for PCM coatings. The solid coating is a combination of polyacrylic matrix with highly dispersed microencapsulated PCM regions. This article evaluates PCM-coated copper substrates fabricated at a total thickness of 1 mm or less.

THE PHASE CHANGE PROCESS

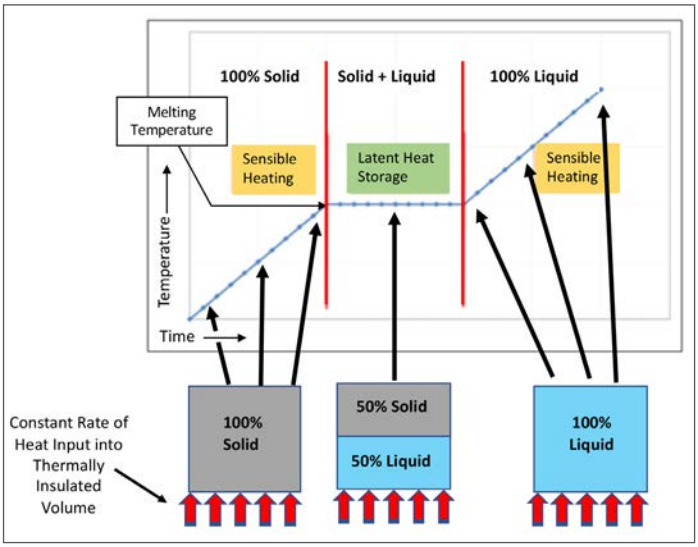

Figure 1. Equilibrium PCM Temperature Curve.

Figure 1 illustrates the effect of a constant rate of heat flow into an otherwise thermally insulated volume of a PCM. The time history of this sample can be divided into three different stages. In the first and third stages, the material is entirely in a single phase: in the first stage, the material is 100% solid. In the third stage, it is 100% liquid. Note, however, that in stages 1 and 3, the tempera-

Mark Hartmann
Mark Hartmann has been polymer and thermal management composite developer for the last 20 years when he joined Outlast Technologies. These materials include the incorporation of the phase change materials and thermally conductive components into textiles, industrial and electronics applications. He is currently CTO of Latent Heat Solutions LLC (LHS). LHS is the renamed industrial focused company after the divesture of the Outlast Technologies textile business.

ture rises linearly under the influence of the constant rate of heat flow. This is the result of what is called "sensible" heating of the material *Equation 1* relates the rate of change in temperature of the PCM to the rate of heat input:

$$\frac{\Delta T}{\Delta t} = \frac{1}{V * \varrho * C_p} * \frac{\Delta Q}{\Delta t} \quad (1)$$

where, $\Delta T/\Delta t$ = °C/sec, V = Volume (cm3), ϱ = mass density (g/cm3), C_p = specific heat at constant pressure (J/g/K), $\Delta Q/\Delta t$ = P_{Heater} = J/sec = Watt.

Once the melting temperature, T_{Melt}, has been reached at the end of stage 1, the PCM begins to liquify, and becomes 100% liquid at the end of stage 2. The temperature remains equal to T_{Melt} throughout stage 2. Any thermal energy flowing at a constant rate into the PCM melts the PCM at a rate determined by *Equation 2*:

$$\frac{\Delta M}{\Delta t} = \frac{1}{L} * \frac{\Delta Q}{\Delta t} \quad (2)$$

where M = mass (g) of liquid PCM, and L = specific latent heat of fusion (J/g). Clearly, the greater the total mass of PCM, the longer it would take to melt the PCM at a specified rate of heat generation.

The amount of heat required to heat up the sample from an initial temperature T_1, which is lower than the melting temperature, and then melts all of the material is:

$$\Delta Q_{Melt} = V * \varrho * [C_p * (T_{Melt} - T_1) + L] \quad (3)$$

The time required to complete the above process equals ΔQ_{Melt} (determined by *Equation 3*) divided by the power:

$$\Delta t_{Melt} = \Delta Q_{Melt} / P_{Heater} \quad (4)$$

The above analysis, indicates that, once the temperature of the PCM reaches the melting temperature, T_{Melt}, this melting process serves to moderate temperature increases in a component in thermal contact with it. However, once the PCM is entirely liquid, its ability to moderate temperature increases in the component ceases, apart from the relatively small energy absorption associated with its specific heat. Hence, in the application of PCMs, it is important to have an estimate of how long it would take for the PCM to become entirely liquified so that this condition could be avoided as much as possible in the application.

In actual applications, the PCM is not thermally isolated, but, rather, it is configured to transfer heat to the ambient to extend the time before the PCM completely melts. Hence, the value of ΔT_{Melt} determined by the above procedure for a thermally isolated PCM would represent a lower bound compared with the typical situation in which heat is lost to the ambient. Nevertheless, despite its approximate nature, the above calculation has value because of its simplicity.

PCM COMBINED WITH COPPER SHEET AND FOIL.

Experimental Method:

A test apparatus thermal kit (*Figure 2*) was designed using a 2-W, 4-ohm wire-wound resistor (5 mm X 10 mm) attached to an isolated FR-4 PCB (7.2 cm X 9.5 cm) placed in a controlled-environment sealed container (14.5 cm X 14.5 cm X 16.5 cm) and centrally positioned. A small 10 mm x 10 mm copper plate of 550 µm thickness was attached to the resistor using a thermally conductive epoxy adhesive. A thin thermocouple was attached to the side of this small plate as the embedded thermocouple. A regulated DC power supply [2] operating at 3.0 V and 0.78 A produced a constant power output of 2.4 W. Heat spreader samples were attached to the heating element using small amount of thermal compound [3] and were approximately 8 mm above the PCB. These temperatures were presumed to be more indicative of the effect that materials would have on a realistic heating point, i.e. CPU, resistors, etc.

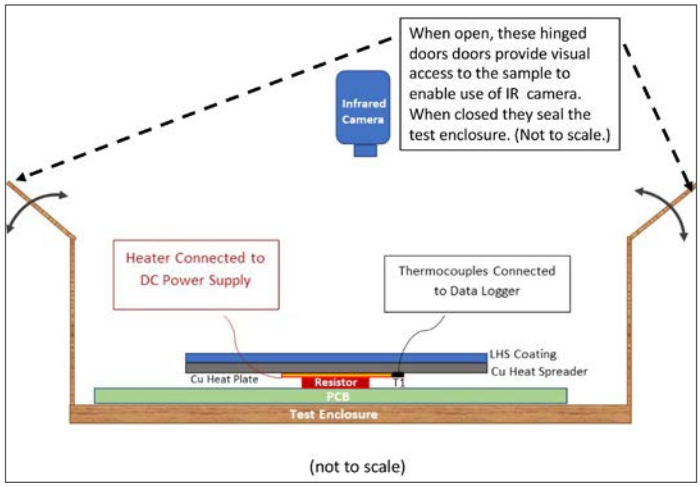

Figure 2. Test apparatus with heat spreader sample.

Thermal images were obtained with a commercial infrared (IR) camera [4] immediately after opening the enclosure by the IR camera positioned over the enclosure. The various experimental samples are described in *Table 1*, which provides details of the sample construction, the material properties, and critical dimensions.

Copper foil and sheet heat spreaders were made of 99+% pure material. The coating was a combination of polyacrylic matrix with microencapsulated C_{20} (Eicosane) PCM. The PCM had a phase change temperature of 36-37°C. The polymer matrix encapsulated the PCM and mitigated the effects of bulk volume changes of the PCM during its solid-liquid phase transition. The LHS coating had a specific latent heat of fusion of 120-130 J/g and a specific heat of 2.1-2.2 J/g·K.

TABLE 1

Heat Spreader Construction, Material Properties, and Dimensions

Sample Type	Metal Substrate			Coating					Sample	
	Material	Thermal Conductivity Range	Thickness	Material	Avg. Thickness	Areal Density	Thermal Conductivity Range	Phase Change Temp. Range	Avg Total Thickness	Mass
		(W/m-K)	(μm)		(μm)	(gm/cm²)	(W/m-K)	(°C)	(μm)	(gm)
1	Cu	360-370	50	N/A	N/A	N/A	N/A	N/A	50	1.12
2	Cu	360-370	550	N/A	N/A	N/A	N/A	N/A	550	12.32
3	Cu	360-370	50	PCM coating	515	0.049	0.30 - 0.35	36-37	565	2.35
4	Cu	360-370	50	PCM coating	945	0.093	0.30 - 0.35	36-37	995	3.45

All Samples are square, side length = 50 mm

Table 1. Heat Spreader Construction, material Properties, and Dimensions.

The experimental setup was designed under the assumption that the energy source to be cooled has an area of contact significantly less than the overall surface area of the heat spreader. Thus, by taking advantage of the available volume in the device beyond the component to be cooled, a much greater volume of PCM can be put in thermal contact with the energy source while keeping the overall thickness of the PCM coated heat spreader less than or around 1 mm.

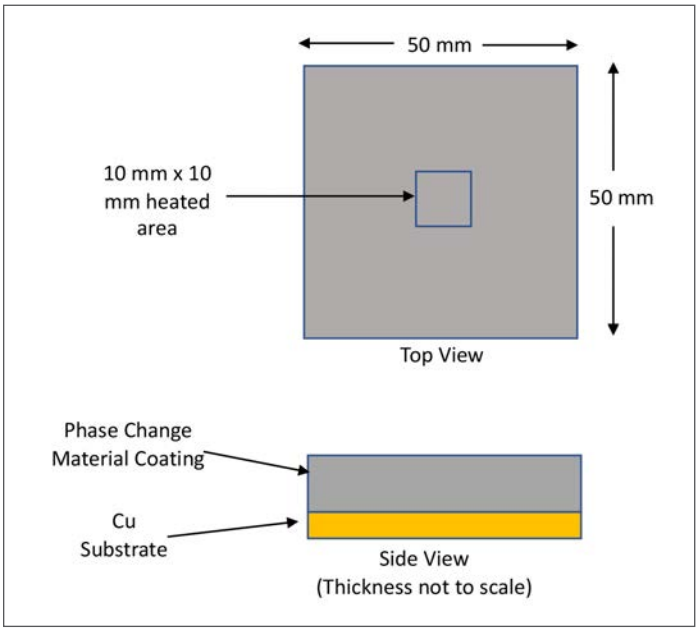

Figure 3. Depicts the design of a typical sample evaluated in this study. It consists of a copper substrate with a solid PCM coating layer.

Figure 3 depicts the design concept for the samples evaluated here. It consists of coating a copper substrate with a PCM coating layer of a solid form of the PCM.

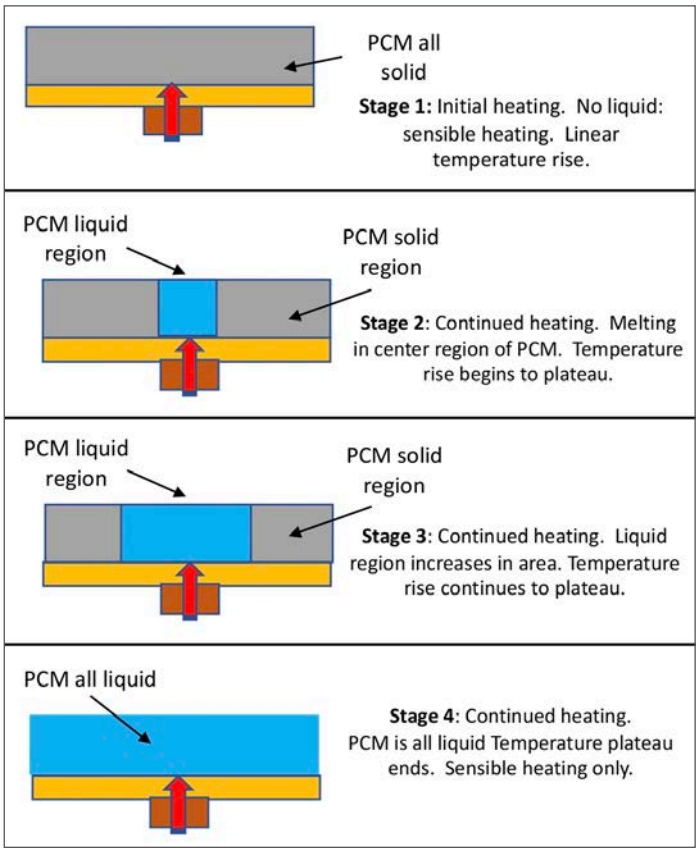

Figure 4. Depicts the different stages of the phase change in a solid coating on a heat spreader with a centrally located heat source much smaller in extent than the substrate. The molten region of the PCM is initially created in the center. Over time, it spreads radially until the PCM everywhere in the sample becomes molten. The IR images in Figure 5 illustrate this process vividly and show clearly the radial spreading of the molten region of the PCM.

Figure 4 depicts the different stages of the phase change in a solid

coating on a heat spreader with a centrally located heat source much smaller in extent than the substrate. One notes that the solid-liquid interface travels radially outward from the heated region in the center of the sample.

The IR images in *Figure 5* illustrate this process quantitively by virtue of the fact that the liquid phase exists in a narrow temperature range and, hence, appears as an isothermal region, in this case, identified by a red color in the image. Also, one should keep these 4 phases in mind when interpreting the temperature profiles in *Figure 6*.

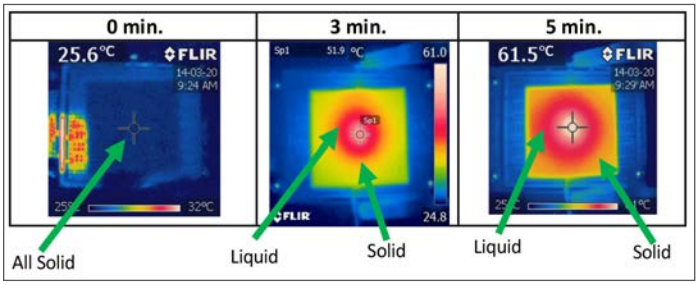

Figure 5, IR Images–Sample 3. 50 µm Cu foil with 565 µm avg. thickness PCM coating. Measured at 2.4W constant power input. Due to the small melting range (36-37°C) the liquid region of the PCM appears to be isothermal and is colored red. This behavior should be compared with the temperature profile for this sample in Figure 6.

DISCUSSION

Figure 6 shows the temperature profiles of the two copper heat spreader control samples and two PCM-coated samples. These four samples were evaluated to show the variables of a) improved thermal conductance of thicker copper (50 µm copper foil versus 550 µm copper sheet), and b) temperature delay/plateauing benefits of a PCM coating on a copper heat spreader, due to the effect of latent heat thermal energy storage.

The standard copper materials (Samples 1 and 2), without any PCM, performed as expected, where the samples exhibit monotonically increasing temperatures, as is typical for a sensible heating process. There are no phase transitions that would result in plateaus in the heating curve. The copper foil, which has the least mass, had the fastest rate of temperature increase and the highest steady-state temperature, the result of having a lower heat spreading ability. The thicker, higher mass 550 µm copper sheet, had lower rate of temperature increase due to its higher mass and a slightly lower steady-state temperature (84°C versus 72°C), due to its greater heat spreading ability.

The temperature profiles for Samples 3 and 4 show the temperature curves of the two coated-copper-foil samples. These two coated samples are interesting in that when additional material was added to the 50 µm copper foil, they perform comparably or better than the thicker, higher-mass copper 550 µm sheet, by exhibiting a reduced temperature during the transient stage and a delay in reaching the steady-state stage.

As the materials approach the 10-minute time, the phase change in Sample 3 is mainly complete and is slowly approaching steady state. Sample 4, due to its higher mass of PCM and associated total latent heat, is not completely phase changed and yields lower temperatures, further delaying full steady state conditions.

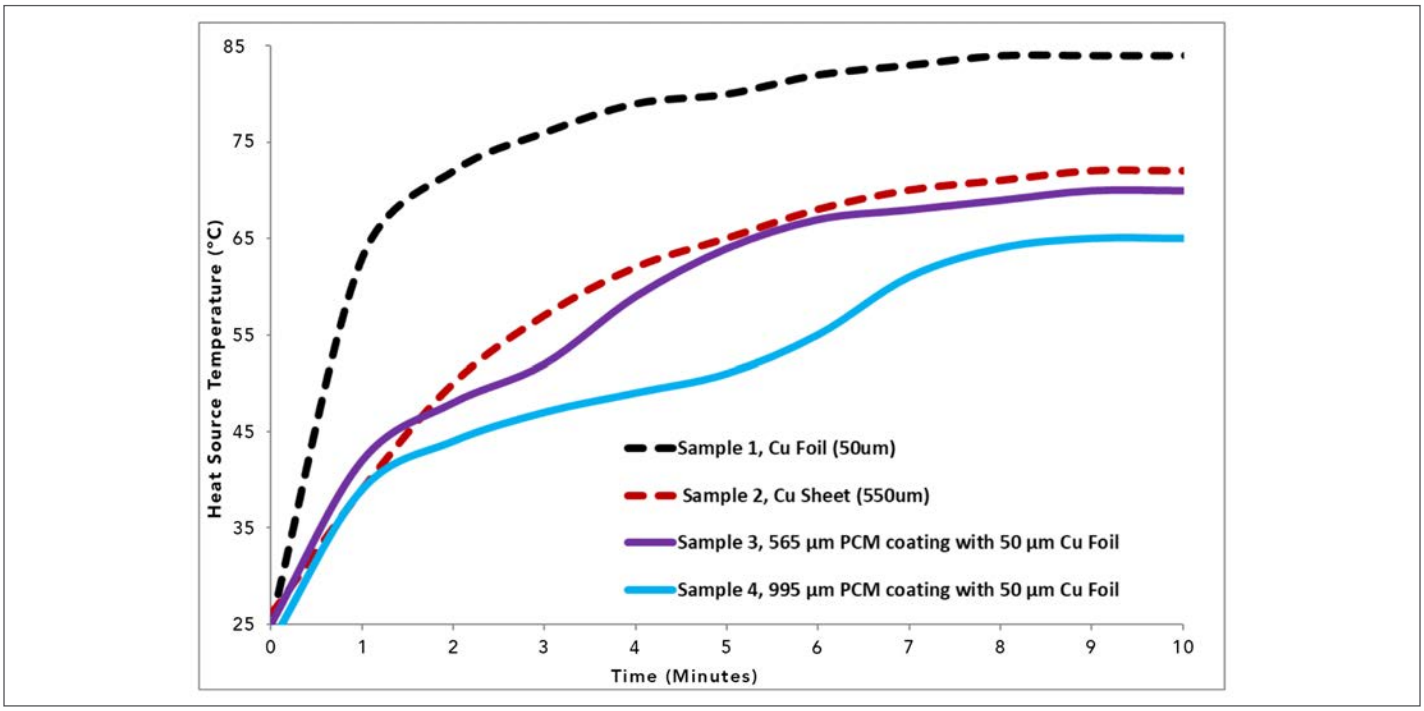

Figure 6. Temperature Profiles for uncoated and PCM coated copper heat spreaders, Samples 1 – 4. Conditions: 2.4W constant power for 10 minutes. Ambient temperature = 25°C.

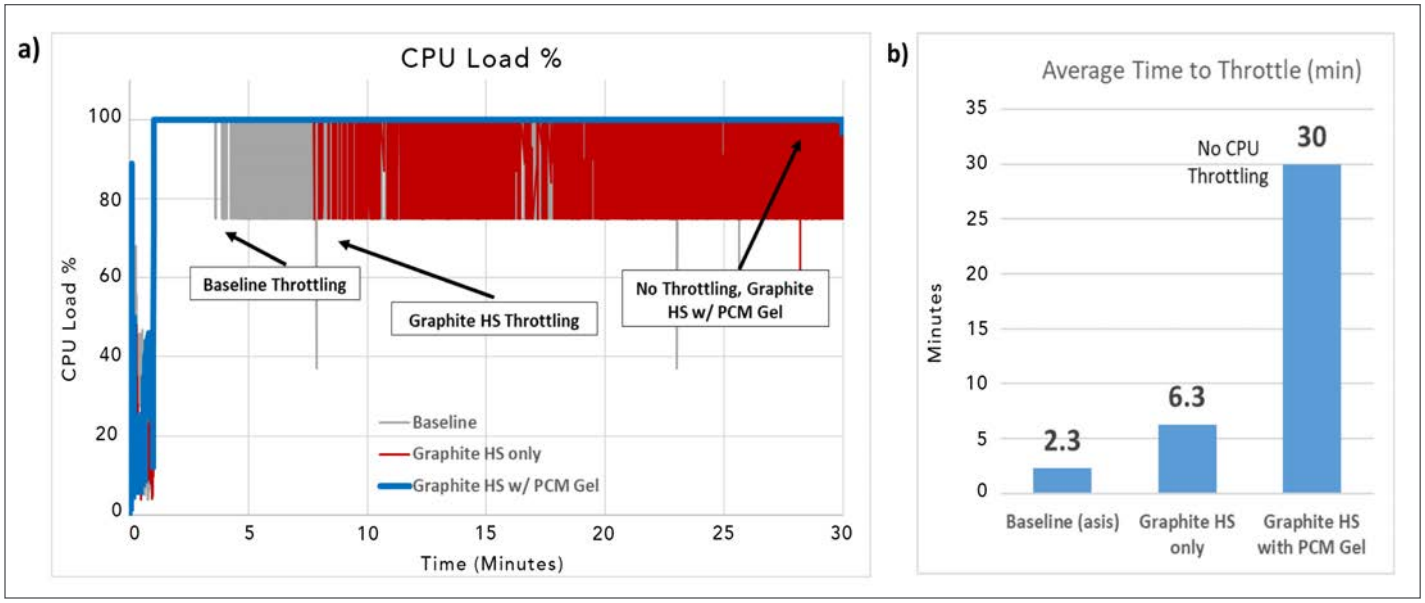

Figure 7. CPU behavior in a commercial tablet device indicating the extent of performance throttling for 3 different heat spreader configurations: 1) baseline case (no heat spreader), 2) 25 µm thick graphite heat spreader only (no PCM), and 3) 25 µm thick graphite heat spreader with a 1 mm PCM coating. Figure 7a: graph illustrating periods of throttling for the three cases. Figure 7b: graph quantifying the number of minutes of operation before the onset of throttling for each of the three cases.

It is worth comparing the values of Δt_{Melt} calculated for Samples 3 and 4 using *Equations 3* and *4*, assuming thermally isolated PCMs, and values of T_i and T_{melt} equal to 25°C and 36.5°C, respectively. The results are: Sample 3,761 sec (12.7 min) and Sample 4, 1,444 sec (24.1 min.) These calculations are consistent with the observed time/temperature behavior. Sample 3 appeared to be approaching steady state at the 10 minute mark. On the other hand, at this same value of elapsed time according to the calculations, in Sample 4 less than half of the PCM had undergone a phase transition into the liquid state. These results demonstrate the utility of these simple calculations in providing a lower-bound estimate for how long it will take for a given PCM to completely liquify.

Therefore, PCMs provide their optimum benefits in applications with transient power loads where the PCM and heat spreader are optimized for the application requirements and device design. This can include adjusting PCM phase change temperature, amount, placement in the device along with varying heat spreader material and size. Continuing this concept, various configurations of heat spreaders and PCMs were tested in a commerical tablet device. *Figures 7a* and *7b* show the average time to CPU throttling and the CPU load percent in a tablet when optimized systems are utilized. The tablet was analyzed for 30 minutes under Dhrystone [5] conditions with a 25 µm graphite heat spreader combined with a 1 mm PCM gel. The PCM heat spreader was positioned between the electronics and back cover with graphite heat spreader side covering the full area of the electronics (10.5 cm X 15.3 cm). These results show that for a 30-minute run time, the device with the PCM heat spreader experienced no throttling at all. In comparison, the table with no heat spreader experienced 27.7 minutes of CPU throttling and the tablet with a heat spreader but no PCM had 23.7 minutes.

CONCLUSION

The above experiments demonstrate an effective method of improving the performance of heat spreaders for mobile devices. The addition of latent heat absorption coatings provides significant benefits by increasing the efficiency of thinner, lower-mass heat spreader materials to make their thermal performance comparable to thicker, heavier materials without these coatings. The use of lighter PCM-coated heat spreaders has both economic and weight benefits, and produces systems with lower peak transient temperatures, leading to improved-performance electronics by reducing CPU throttling. PCM coatings combined with high conductivity (>1,000 W/m·K) graphite heat spreaders and used in mobile devices provide for improved CPU performance and lower battery temperatures. When combined with electrically insulative 170 W/m·K aluminum nitride heat spreaders, these can be downsized for electronics and LED applications.

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[2] Digi 35A DC Power Supply, mfg. by Electro Industries Inc.

[3] Artic Silver 5 mfg. by Artic Silver Inc.

[4] FLIR i7 Thermal Imaging Camera, mfg. by FLIR Systems, Inc.

[5] https://en.wikipedia.org/wiki/Dhrystone

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A fellow of the American Society of Mechanical Engineers (ASME) since 2014, Dr. Victor Adrian Chiriac is the principal architect and U.S. thermal technology lead for mobile devices in Futurewei Technologies (Huawei R&D USA). Victor was elected Chair of the ASME K-16 Electronics Cooling Committee and was elected the Arizona and New Mexico IMAPS Chapter President. He is a leading member of the organizing committees of ASME/InterPack, ASME/IMECE and IEEE/CPMT ITherm Conferences. He holds 16 U.S. issued patents and has published over 107 papers in scientific journals.

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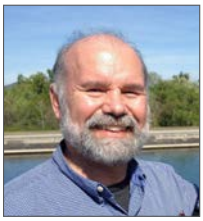

BRUCE GUENIN | CONSULTANT

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Dr. Bruce Guenin has spent many years in the electronics and computer industries, which has given him a broad perspective on macro trends in these fields. He has been an editor of *Electronics Cooling*® since 1997 and has contributed, to date, 35 installments of the tutorial column, Calculation Corner. His previous affiliations include Oracle, Sun Microsystems, and Amkor. He is a past chairman of the JEDEC JC-15 Thermal Standards Committee and the Semi-Therm® Conference. His contributions to the thermal sciences have been recognized by receiving the Harvey Rosten Award in 2004 and the Thermi Award in 2010 from the Semi-Therm® Conference. He received the B.S. degree in Physics from Loyola University, New Orleans, and the Ph.D. in Physics from the University of Virginia. He has authored and co-authored over 80 papers and articles in the areas of thermal and stress characterization of microelectronic packages, electrical connectors, solid state physics, and fluid dynamics and has been awarded 18 patents in these areas.

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Short Courses Monday March 16, 2020

Micro-Two-Phase Electronics Cooling…Getting It On Its Way
John R. Thome, EPFL

Two-phase flow and flow boiling heat transfer can reliably cool heat fluxes in excess of 500 W/cm2 with heat transfer coefficients nearing 100 kW/m2K with respect to the cold plate's base area. Yet, industry is hesitant to accept this technology on a large scale. Most of the reservations about this approach are easily mitigated with proper design/planning, and the benefits are substantial. In general, a micro-thermosyphon that works passively with gravity-driven flow is used with heat dissipation to a compact air coil. Due to the new "form factor" and huge surface area of the coil compared to an air-cooled heat sink, energy consumption by the fans is greatly reduced. Furthermore, a thermosyphon (no electrical driver or flow controllers) provides high reliability that is commonplace with packages which use two-phase thermal management. This lecture will recount the history and background of two-phase cooling, noting lessons learned along the way. Several case studies will be presented where a design flaw was mitigated and the resulting improvements in performance will be highlighted. At the end of this course, you will be able to successfully design a two-phase cold plate cooled system which improves the reliability, cost of operation, and longevity of your devices.

John R. Thome is Professor-Emeritus of Heat and Mass Transfer at the Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland since 1998. He obtained his Ph.D. at Oxford University in 1978. Having retired in July 2018 at the EPFL, he co-owns the consulting/thermal engineering software company, JJ Cooling Innovation Sàrl in Lausanne. He is also a Visiting Professor at Brunel University in London and an Honorary Professor at the University of Edinburgh…to keep his "feet" in research while still supervising MS student theses at the EPFL. He recently received the 2019 IEEE Richard Chu ITHERM Award for Excellence in Thermal and Thermo-Mechanic Management of Electronics and the 2019 ASME Allan Krause Thermal Management Medal at InterPack. He is the author of five books on two-phase heat transfer and flow and has over 245 journal papers on macroscale and mircoscale two-phase flow, flow visualization, boiling/condensation heat transfer, flow pattern-based models, and micro-two-phase cooling systems for electronics cooling. He has done numerous sponsored projects with IBM, ABB, Nokia Bell Labs, Carl Zeiss, CERN, etc. He is editor-in-chief of the 16-volume series Encyclopedia of Two-Phase Heat Transfer and Flow (2016-2018). He founded the Virtual International Research Institute of Two-Phase Flow and Heat Transfer in 2014, now with 25 participating universities to promote research collaboration, sharing of experimental and numerical data, and education.

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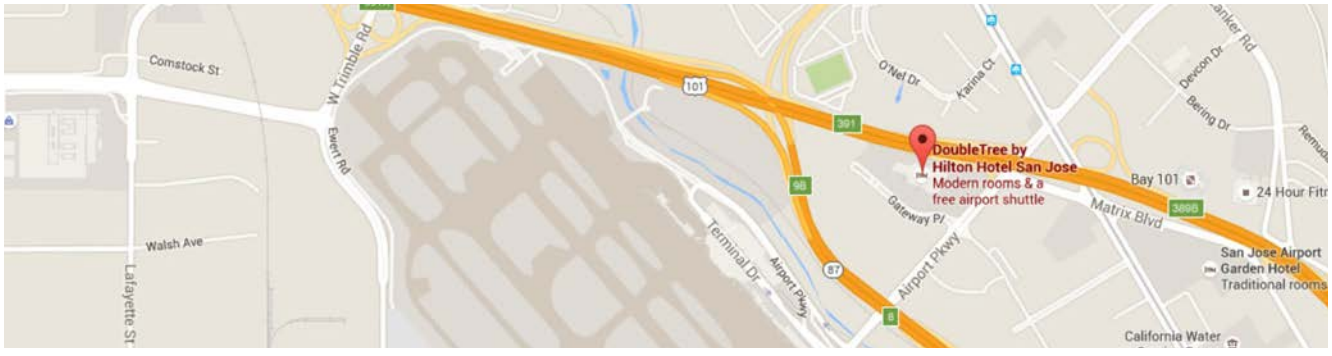

Short Courses Monday March 16, 2020

Let's Work Together: How Co-Design Leads to Better Solutions in Thermal Management
Lauren Boteler, Army Research Laboratory

Optimization studies are generally done intradisciplinary rather than interdisciplinary, and this leads to conflict as different fields have different values when it comes to what they want in a packaged solution. Heat sinks in energy dense power electronics are an excellent example of where better communication and co-design models can yield significant improvements to fielded performance with just a small amount of preparation during the design phase. Parameterization and Figure of Merit (FOM) definitions that encapsulate electrical/thermal/mechanical properties pare down the solution space to a set that represents what all fields want rather than cyclically proposing "optimal" solutions that one or more fields can't possibly accommodate. This course will examine how fielded solutions were truly optimized using novel co-design tools and optimization techniques which span multiple disciplines. The case studies examined will show marked improvement beyond what single-track minded approaches yield, and lessons learned from this course will translate directly to better solutions in your workplace.

Dr. Lauren Boteler leads the thermal and packaging research programs as part of the Advanced Power Electronics group at the U.S. Army Research Laboratory (ARL). She received her Ph.D. degree in mechanical engineering from the University of Maryland. Her work at ARL, beginning in 2005, has focused on electronics packaging and thermal management solutions for a wide range of Army applications. She designs thermal and packaging solutions including 3D chip stacking, power electronics, laser diodes, RF HEMT devices, top side cooling, phase change materials, and additive manufacturing. More recently, she has initiated a research program in Advanced Power Electronics Packaging and Thermal Management which focuses on four main challenges of power electronics packaging: transient thermal mitigation, additive manufacturing, coengineering/codesign, and high-voltage packaging. She was also awarded the 2018 ASME EPPD Woman Engineer of the Year award for her contributions to the electronics packaging community.

Air Movers and Aeroacoustics for Electronics Cooling
Mark MacDonald, Intel Corporation

This course will survey performance characteristics of various relevant fan types, including axial fans, blowers, crossflow or tangential blowers, volumetric resistance blowers, and other emerging technologies including electronhydrodynamic blowers, synthetic jets, piezo flappers, and micropumps. Emphasis will be placed on understanding the physical mechanisms of operation, best practices for characterization, implementation considerations, and applicable scaling laws (including acoustic scaling laws). The course will also cover aeroacoustics and psychoacoustics (sound quality and ergonomics) for consumer electronics in detail.

Mark MacDonald holds a Ph.D. from Cornell University, and is a Principal Engineer at Intel. An Adjunct Professor at Portland State University, he is the holder of 45 patents, 17 of them specific to air movers, Dr. MacDonald has won the Martin Hirschorn Prize from International Acoustics Congress for work on notebook blower acoustics.

Short Courses Monday March 16, 2020

Introduction to Electronics Cooling
Patrick Loney, Northrop Grumman Mission Systems

As electronic packages get smaller and the power dissipations increase, performing robust thermal analyses is an increasingly important step in the electronics packaging design process. This course will focus on the component level of the electronics assembly. Thermal management, proper cooling techniques, component attachment, and analytical modeling methods will be presented. How to decipher vendor datasheets will be discussed as well as the basics of how to model custom components. Best practices for steady state and transient operational modes are included. Process development will also be presented along with discussions on requirements compliance. Students will finish the course with an understanding of how to determine the limits and requirements of an electronics component, assess the thermal performance, how to integrate the performance model into a Next Higher Assembly (NHA) thermal model, and most importantly, how to communicate this information to their internal and external customers who are dependent on this data.

Patrick Loney recently celebrated his 30th anniversary with Northrop Grumman Corporation. He has over 35 years of experience in the thermal engineering/electronics cooling industry. He received his Batchelor of Sciences degree in Nuclear Engineering from the University of Illinois and his Masters of Sciences degree in Mechanical Engineering from Cleveland State University. He holds several US Patents and Trade Secrets, mostly dealing with thermal management and electronics cooling techniques. He has presented similar courses to internal customers as well as the 2019 IPC AMEX Expo.

Introduction to Thermal Modeling with OpenFOAM
John F. Maddox, University of Kentucky

OpenFOAM is the leading free, open source software for computational fluid dynamics (CFD). This course is an introduction to thermal modeling using OpenFOAM for users familiar with CFD and heat transfer, however, no prior experience with OpenFOAM is required. Attendees will be introduced to the OpenFOAM environment through hands-on tutorials covering meshing, solving, and post-processing with a focus on conjugate heat transfer. Attendees wishing to participate in the hand-on tutorials will need to bring a laptop with a 64-bit operating system (Window, Mac, or Linux) and Oracle VM VirtualBox installed. All the software required for this course will be free and open source.

Dr. John F. Maddox is an Assistant Professor of Mechanical Engineering at the University of Kentucky, Paducah Campus. He received his Ph.D. in mechanical engineering from Auburn University in 2015. His primary research areas are thermal management of high power electronics through jet impingement and thermal characterization of advanced materials used in aerospace and electronics cooling applications.

Design And Optimization Of Heat Sinks

Marc Hodes and Georgios Karamanis, Transport Phenomena Technologies, LLC

This course provides the audience with an understanding of heat sink design and optimization in the context of the thermal management of electronics. The course has two parts. The first part begins with an overview of common methods to manufacture heat sinks such as extrusion, die casting and forging, and discusses their advantages and disadvantages with respect to cost and fin geometry. Attention then shifts to the theory of spreading resistance and how it can be calculated in order to properly size the thicknesses of the bases of heat sinks. Next, the theory of the operation of heat pipes in tubular and flat (vapor chamber) configurations is presented along with their roles in smoothing out temperature gradients in the fins and bases of heat sinks. In the second part of the course, single-phase conjugate heat transfer, where conduction in the heat sink is coupled to convection in the coolant, i.e., air or water, flowing through the heat sink is highlighted. We discuss why the constant heat transfer coefficient assumption tends to be an invalid one in real heat sinks by using specific examples. Then, the use of computational fluid dynamics (CFD) to compute conjugate Nusselt numbers is considered. The course concludes with a discussion of how to embed pre-computed results for conjugate Nusselt numbers and dimensionless flow resistances for heat sinks in flow network models (FNMs) of circuit packs such as blade servers. Finally, how to use a multi-variable optimization scheme to optimize the geometry (fin thickness, spacing, height, length, say) of an array of heat sinks in a circuit pack represented by an FNM model with embedded tabulations of CFD results is discussed.

Dr. Marc Hodes is a Professor of Mechanical Engineering at Tufts University and the CTO of Transport Phenomena Technologies, LLC. He received his B.S., M.S. and Ph.D. degrees in Mechanical Engineering, the latter from MIT in 1998. He held a succession of appointments at Alcatel-Lucent's (now Nokia's) Bell Laboratories from Postdoctoral Scientist to Manager of a Thermal Management Research Group between 1998 and 2008, when he joined Tufts University.

Dr. Georgios Karamanis is a Co-Founder and Senior Engineer at Transport Phenomena Technologies, LLC. He received his Ph.D. and M.S. in Mechanical Engineering from Tufts University. He has expertise in analytical, numerical and experimental techniques relevant to convective transport. He is the PI in a NSF Phase I SBIR awarded to Transport Phenomena Technologies, LLC, to develop specialized thermal modeling software for Data/Telco centers.

Keynote Speaker

Andy Delano, Microsoft

Andy Delano leads the Microsoft Surface team's thermal architectural efforts primarily focusing on the Pro product line. Prior to joining Microsoft in 2012, Andy managed an R&D team within Honeywell's Specialty Materials division developing and launching highly successful products for the electronics packaging industry. Andy started his career in 1998 as a thermal engineer at Hewlett-Packard working on enterprise server and workstation thermal design. While at HP, Andy was also an adjunct professor at CU and taught heat transfer, thermodynamics, and thermal systems design between 1999 and 2005. Andy obtained his Ph.D. In mechanical engineering from Georgia Tech in 1998 and his thesis was on a single pressure absorption refrigerator originally patented by Albert Einstein. During the first part of his graduate studies, Andy also worked on the design and production of the 1996 Olympic Torch and spent 6 weeks traveling with the torch relay.

Luncheon Speaker

Bletchley Park: Enigma, Ultra, and the Making of Colossus
The Development of the First Digital Computing Systems

Presenter: David L. Saums, DS&A LLC

This presentation will outline the breaking of the German Enigma code (which became a series of different codes, used by different armed forces services), which produced what was titled as top-secret "Ultra" information about German military plans, locations of ships and submarines and battle groups, and how these first mechanized codebreaking machines were devised.
The presentation will focus on the technologies employed and short descriptions of hardware developed, as precursors to the modern age of digital computing – but will also illustrate the human contributions to preventing the destruction of the modern democratic world in the 1940s. The connections to technology in today's world arose from what would otherwise have been the ashes of defeat.

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