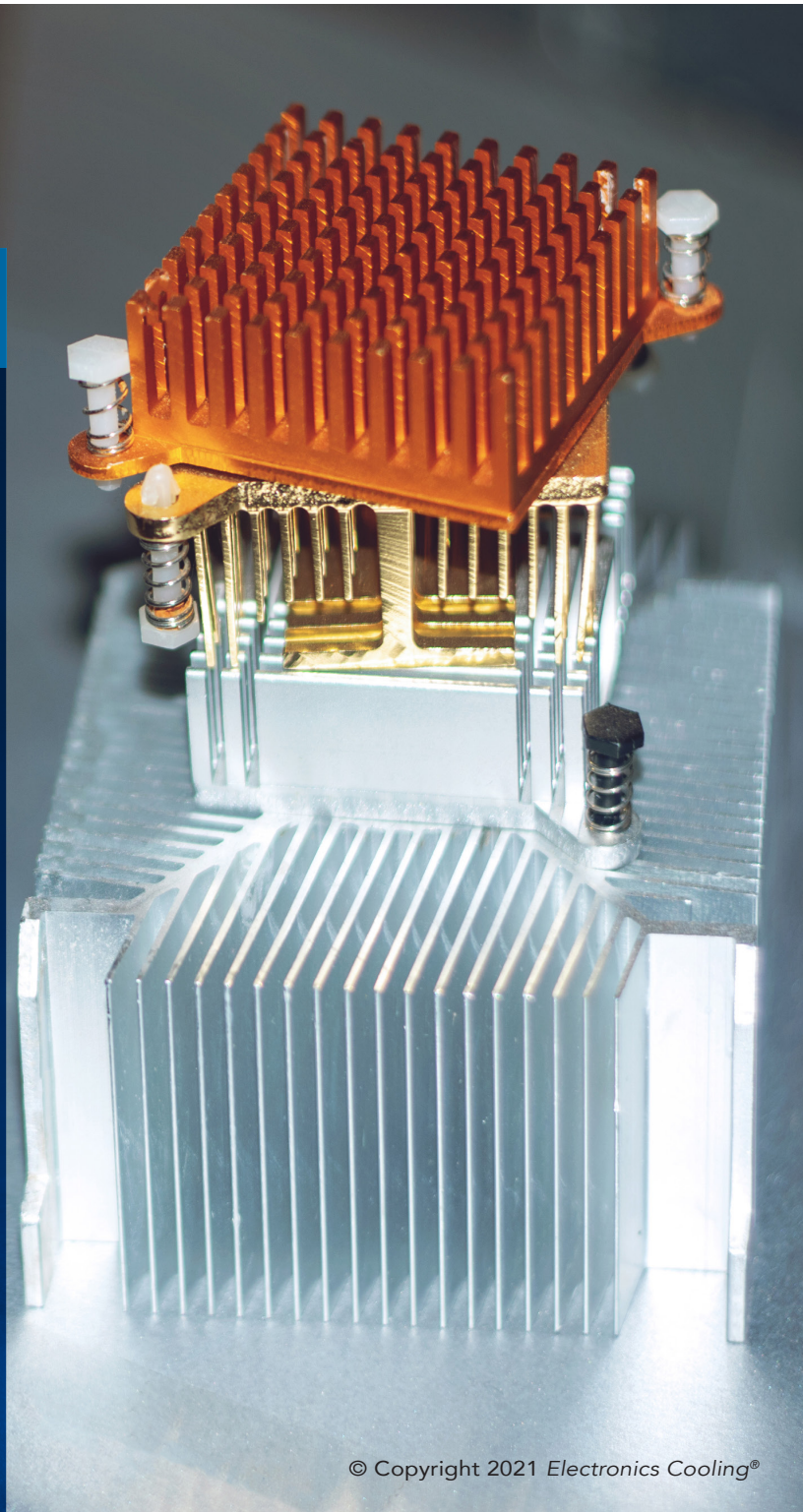
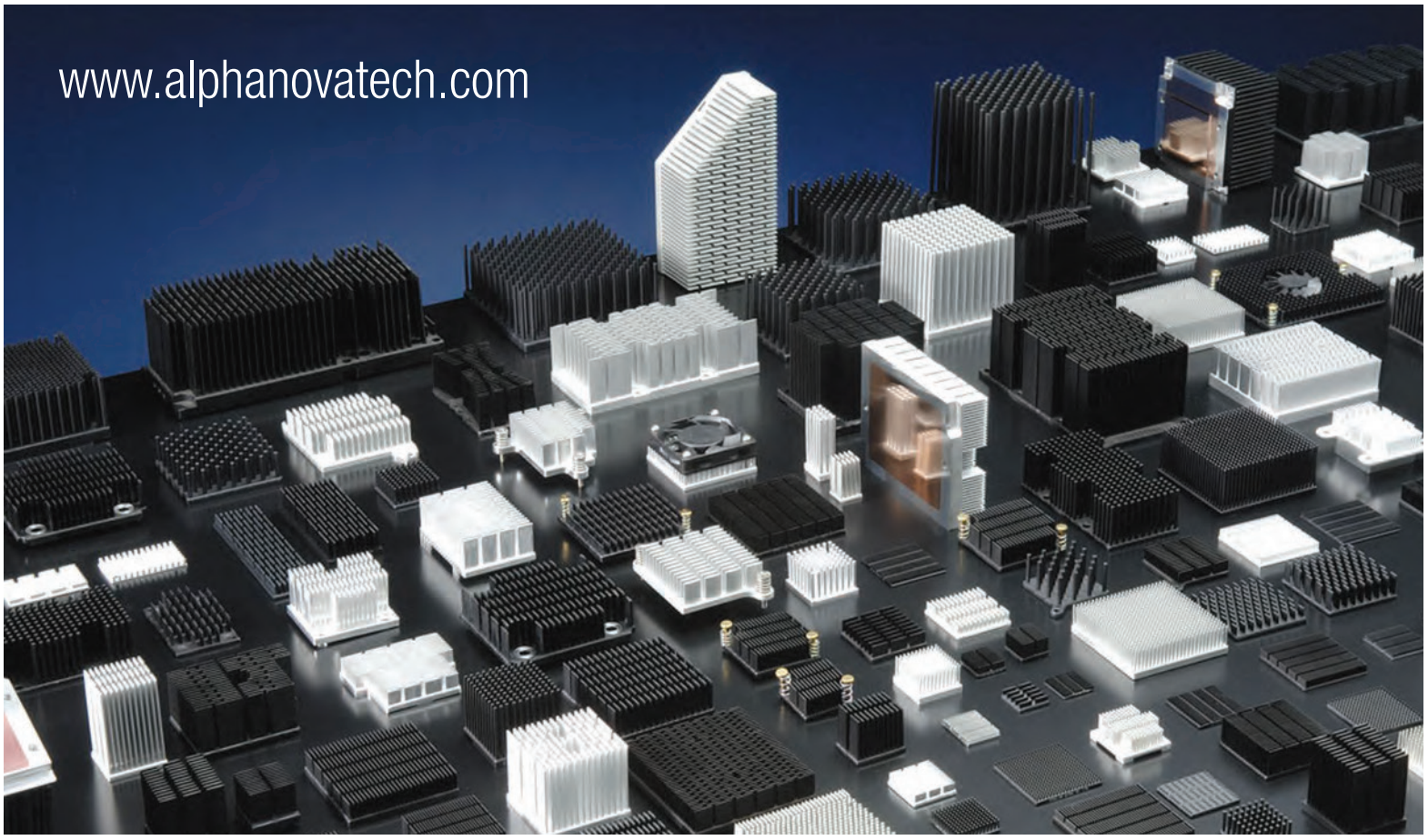
FALL 2021
electronics-cooling.com

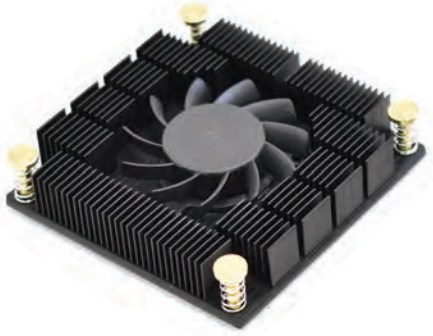
electronics COOLING

FEATURED IN THIS EDITION





Alpha's Extensive Products and Services



ALPHA Co., Ltd.
Head Office
www.micforg.co.jp

256-1 Ueda, Numazu City, Japan 410-0316
Tel: +81-55-966-0789 Fax: +81-55-966-9192
Email: alpha@micforg.co.jp

ALPHA NOVATECH, INC.
USA Subsidiary
www.alphanovatech.com

473 Sapena Ct. #12, Santa Clara, CA 95054 USA
Tel: +1-408-567-8082 Fax: +1-408-567-8053
Email: sales@alphanovatech.com

ALPHA | Your partner for thermal solutions

CONTENTS

electronics COOLING
www.electronics-cooling.com

PUBLISHED BY
Lectrix
1000 Germantown Pike, F-2
Plymouth Meeting, PA 19462 USA
Phone: +1 484-688-0300; Fax:+1 484-688-0303
info@lectrixgroup.com
www.lectrixgroup.com

CHIEF EXECUTIVE OFFICER
Graham Kilshaw | Graham@lectrixgroup.com

VP OF MARKETING
Geoffrey Forman | Geoff@lectrixgroup.com

EDITORIAL DIRECTOR
James Marengo | James@lectrixgroup.com

BUSINESS DEVELOPMENT DIRECTOR
Janet Ward | Jan@lectrixgroup.com

CREATIVE DIRECTOR
Chris Bower | Chris@lectrixgroup.com

SENIOR GRAPHIC DESIGNER
Kate Teti | Kate@lectrixgroup.com

CONTENT MARKETING MANAGER
Danielle Cantor | Danielle@lectrixgroup.com

ADMINISTRATIVE MANAGER
Eileen Ambler | Eileen@lectrixgroup.com

ACCOUNTING ASSISTANT
Susan Kavetski | Susan@lectrixgroup.com

►**SUBSCRIPTIONS ARE FREE**
Subscribe online at
www.electronics-cooling.com

For subscription changes email
info@electronics-cooling.com

Reprints are available on a custom basis at reasonable prices in quantities of 500 or more. Please call +1 484-688-0300.

FREE SUBSCRIPTIONS

Lectrix®, *Electronics Cooling®*—The **2021 Fall Edition** is distributed annually at no charge to engineers and managers engaged in the application, selection, design, test, specification or procurement of electronic components, systems, materials, equipment, facilities or related fabrication services. Subscriptions are available through electronics-cooling.com.

LECTRIX®

EDITORIAL

Ross Wilcoxon
Associate Technical Editor

Welcome to the Fall 2021 issue of Electronics Cooling magazine. It seems like it has been a long time since I've had the opportunity to write the editorial – although, in retrospect, anything that happened pre-pandemic seems like a long time ago… My last editorial was written for the Summer 2019 issue and a lot of things have certainly changed in the world since then.

Here in the U.S. at least, there has been some progress in things trending towards 'normalcy'. While the current resurgence in Covid cases has led to considerable uncertainty, we do seem to be ratcheting along a path that will lead to things eventually resembling what they were in the summer of 2019. I don't expect that we will ever go back to things being exactly the same – for example, it is a virtual certainty that many of our meetings will continue to be, well… virtual. But business travel is increasing and it seems reasonable that we will soon attend at least some of our meetings and conferences in person. Having participated in seven virtual conferences or workshops since my last editorial, I am looking forward to (hopefully) attending in-person events in the next few months. One of those events will follow a hybrid format that allows virtual and in-person attendance and I suspect that many of these hybrid events will continue in some form, regardless of the Covid situation. While virtual attendance at a conference does provide some benefits in terms of scheduling and costs, I hope that many attendees choose to attend in person. I know from my experience that the personal connections that I have made while attending conferences have greatly enhanced my professional skills and my ability to work effectively. I hope that the professional growth of future generations of engineers will not be adversely affected by the reduced networking opportunities that are inherent to virtual meetings.

I am excited about this issue of Electronics Cooling magazine, in part because of its focus on design approaches that take advantage of topics such as machine learning, artificial intelligence and additive manufacturing to develop highly optimized designs. These techniques will undoubtedly change how we do things and provide many opportunities for improving designs in unexpected ways. Thermal management is an area that is particularly suitable for taking advantage of these 'generative design' approaches through, for example, novel fin structures that look more at home on a fish than on a heat sink. It is reasonable to expect that these kinds of approaches will increasingly be applied to the design of electronics, which must account for electrical, reliability, SWaP (size, weight and power) in addition to cooling performance.

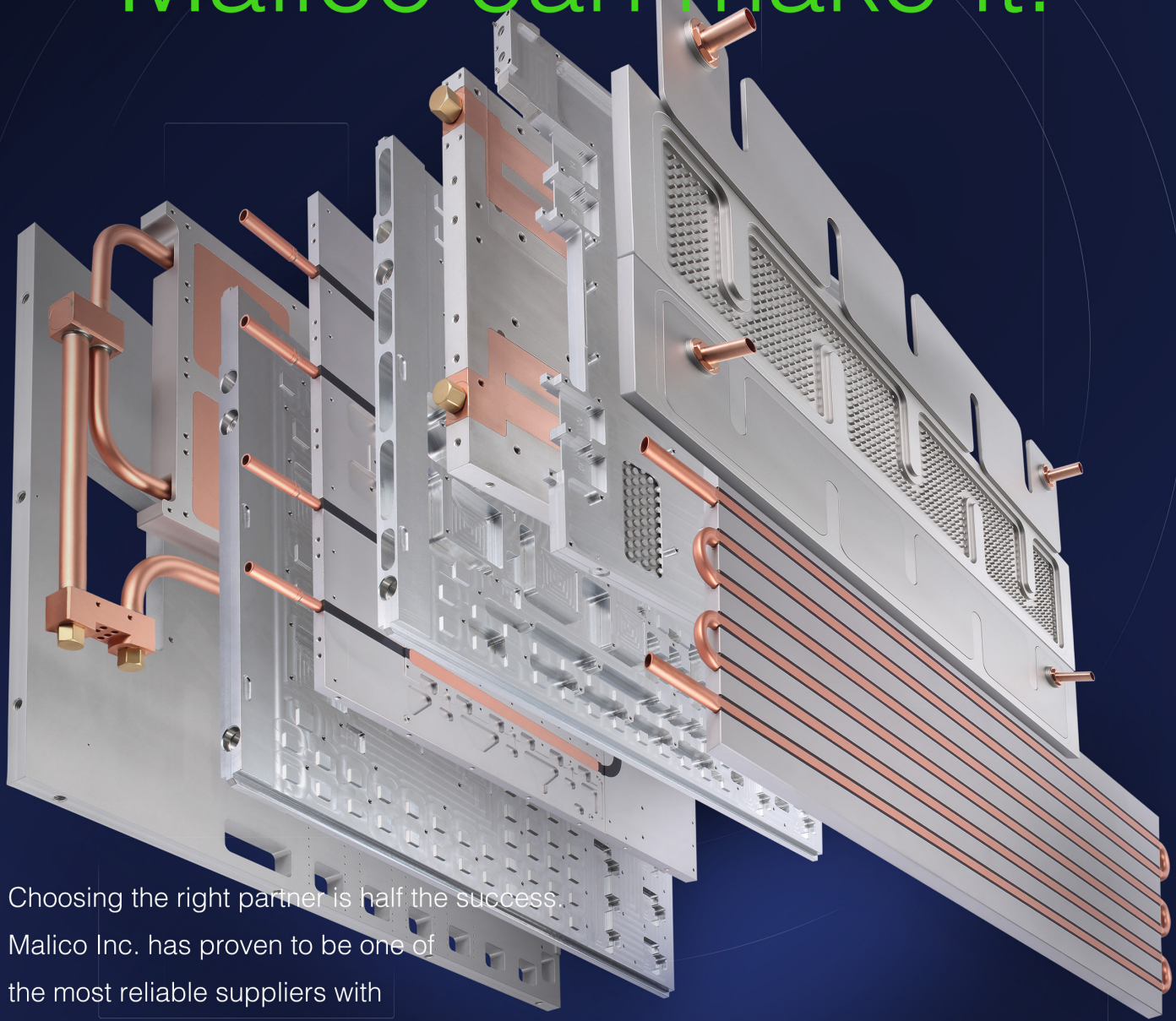
My initial idea for this issue was to focus entirely on generative design, but we editors instead decided that it made more sense to spread the topic across at least two issues. This issue includes two exceptional articles that introduce the topic and provide a clear framework for understanding the challenges to, and approaches in, developing generative designs. In addition, we also have timely articles that describe thermal analysis at both ends of the thermal path (one on component-level design and the other at the system-level) with insight on methods for reducing the complexity of the analysis. In addition, we have a detailed summary of the recent ITherm conference as well a 'Statistics Corner' column that discusses regression analysis.

I hope that you enjoy this issue and welcome any comments or feedback. I also hope to start seeing many Electronics Cooling magazine readers in person at upcoming conferences… eventually…

–Ross Wilcoxon

MALICO INC

If you can design it, Malico can make it.



Choosing the right partner is half the success.
Malico Inc. has proven to be one of
the most reliable suppliers with
the highest quality assurance for over 38 years.

Malico Inc.

www.malico.com

5, Ming Lung Road , Yangmei District ,Taoyuan City ,Taiwan 32663
Tel :886-3-4728155
Fax:886-3-4725979
E-mail:inquiry@malico.com
Website:www.malico.com

COOLING EVENTS

News of Upcoming 2021 & 2022 Thermal Management Events

2021

NOV
15-19

SC21

America's Center | St. Louis, Missouri

The international conference for high performance computing, networking, storage, and analysis. Expand your knowledge, enrich your experiences, and network with others in the HPC community. Take in technical presentations, papers, workshops, tutorials, posters, and Birds of a Feather sessions. Explore exhibits showcasing the latest innovations from the world's leading manufacturers, research organizations, and universities. And, enjoy exploring our host city St. Louis. Journey to the top of the Gateway Arch!

Desc. source: electronics-cooling.com
► https://sc21.supercomputing.org/

2022

JAN
27

THERMAL MANAGEMENT INNOVATION USA

TCF Center | Detroit, Michigan

The Annual BEV Thermal Management Innovation USA Congress, Detroit is the number one event to match buyer requirements with expert solutions during the Automotive sector's battery evolution. Following on from the tremendous success of the previous three events, Thermal Management Innovation USA has firmly established itself as the automotive industries first-class event to gain a clear and pragmatic view of the key challenges and current need to know learning objectives surrounding advanced battery thermal management systems; to increase efficiency, range, battery health, and optimize solutions for increasingly demanding advanced charging requirements.

Desc. source: electronics-cooling.com
► www.battery-thermal-management-usa.com

MAY
10

ThermalLIVE™ SUMMIT

Online Event

The ThermalLIVE™ Summit is a one-day event focused on the latest thermal management breakthroughs, trends and industry developments. With a focus centered on product innovation and technological advancements, the ThermalLIVE™ Summit will offer the latest and greatest content, including whitepapers, videos, and product demonstrations. ThermalLIVE™ 2022 is a two-day, Free online learning and networking event for engineers to learn about the latest topics in thermal management. Produced by *Electronics Cooling*, it showcases the newest techniques and products in the industry.

Desc. source: electronics-cooling.com
► https://thermal.live/

Generative Design for Electronics Cooling

Danny J. Lohan, Yuqing Zhou, and Ercan M. Dede
Toyota Research Institute of North America

INTRODUCTION

Generative design is an iterative design process that involves the use of a *program* to generate a set of *optimized designs* that meet product performance requirements and constraints. Methods that transform statements of performance requirements into product designs are also known as inverse design methods. Associated programs may involve feedback from a human designer or may be completely automated within a computer. Computer-based generative design may use artificial intelligence agents or numerical algorithms including rule-based and physics-driven techniques to generate designs that meet performance requirements. The optimized designs often involve, but are not limited to, product size, shape, or topology, as well as, material and process selection.

The explosion of computing power, discoveries of novel materials, and advancement of manufacturing methods have sparked great excitement over the potential of generative design. New materials (e.g., phase-change polymers) have enabled new product functionalities, and advanced manufacturing processes (e.g., 3D printing) can now make parts we could not imagine manufacturing before. Taking advantage of today's ubiquitous and extremely fast computing power, generative design produces spatially novel yet efficient product designs that can be realized with state-of-the-art materials and manufacturing process capabilities. Today, generative design is not only regarded as an effective tool to reformulate components but an innovative platform to revolutionize product research, development, and design across industries. In this issue and article, the implementation of generative design for electronics cooling applications is discussed.

Danny J. Lohan
Danny received his B.S. degree in general engineering, and his M.S. and Ph.D. in systems and entrepreneurial engineering from the University of Illinois at Urbana-Champaign. Currently, he is a scientist in the Electronics Research Department at the Toyota Research Institute of North America. His research interests include numerical design automation and multi-disciplinary design optimization for electrified systems.

Yuqing Zhou
Yuqing received the B.S. degree in mechanical engineering from Northeastern University, Shenyang, China, in 2012, and the M.S. and Ph.D. degrees in mechanical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2014 and 2018, respectively. He is currently a Research Scientist with the Toyota Research Institute of North America. His research interest is design optimization of Multiphysics systems.

Ercan M. Dede
Ercan received the B.S. and Ph.D. degrees in mechanical engineering from the University of Michigan, Ann Arbor, MI, and the M.S. degree in mechanical engineering from Stanford University, Stanford, CA. He is the Group Manager of the Electronics Research Department at the Toyota Research Institute of North America. His team focuses on systems involving advanced sensors, power semiconductors, and electronics/photonics packaging. He has published over 100 articles on topics related to optimization of thermal, mechanical, and electromagnetic systems. He is one author of a book entitled Multiphysics Simulation: Electromechanical System Applications and Optimization. He holds 135 issued patents.

BIOLOGICALLY INSPIRED DESIGN OF THERMAL CONDUCTORS

In this section, a representative example of how to exploit generative design for a heat transfer (source-to-sink, thermal conductor) application is presented, as explained in detail in [1]. This process includes: 1) identifying a target design space (what type of structure you want to generate); 2) selecting an appropriate design representation (what generative algorithm you wish to use to produce a structure); and 3) utilizing physics-based simulation in an optimization loop to obtain the best performing structure.

Researchers have demonstrated the performance benefits of branching and finned structures for heat transfer applications; see [2, 3] and *Fig. 1* for examples. Nature has spent millions of years fine-tuning the performance of natural branching structures for their respective functions. Using application-relevant observations, design engineers can extract heuristics and embed them into generative design methods to provide an efficient and flexible optimization process. Furthermore, using generative methods, bioinspired characteristics may naturally emerge.

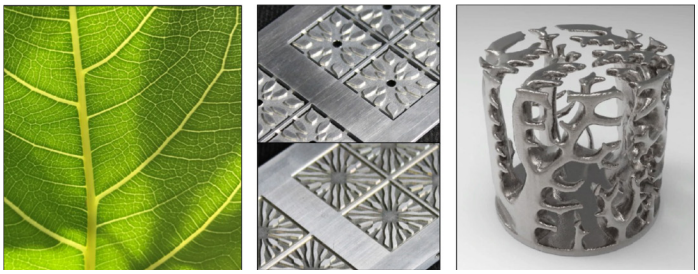


Figure 1. Natural branching pattern (left), branching liquid cooling structures (center) [2], and branching heat sink for natural convection (right, republished with permission of Elsevier Science & Technology Journals, from [3]; permission via Copyright Clearance Center, Inc.).

A survey of algorithms that generate branching structures was performed, including rule-based [4], interaction-based [5], and voxel-based [6] generative algorithms. The reader is referred to [1] for greater discussion of each approach. However, in particular, an interaction-based model called the space colonization algorithm [5], developed to quickly produce trees for computer graphics, was previously selected for further study because it provides a compact design representation (i.e., it requires few design variables), is computationally efficient to generate patterns (i.e., does so in a matter of seconds), and is capable of generating a wide variety of branching structures. The space colonization algorithm is a numerical adaptation of the canalization hypothesis [7], which suggests a theory to model the growth of leaf veins. A sketch of the algorithm is shown in *Fig. 2*. Growth hormone sources called auxins, blue circles, are first introduced onto the domain. Each auxin is paired to its nearest vein node, green circles, to influence its growth direction. The paired vein nodes will then proceed to grow in the average direction of its paired auxins. This process of pairing and growing repeats until all auxins have been reached. With this algorithm, the locations of the auxins are varied to search the design space.

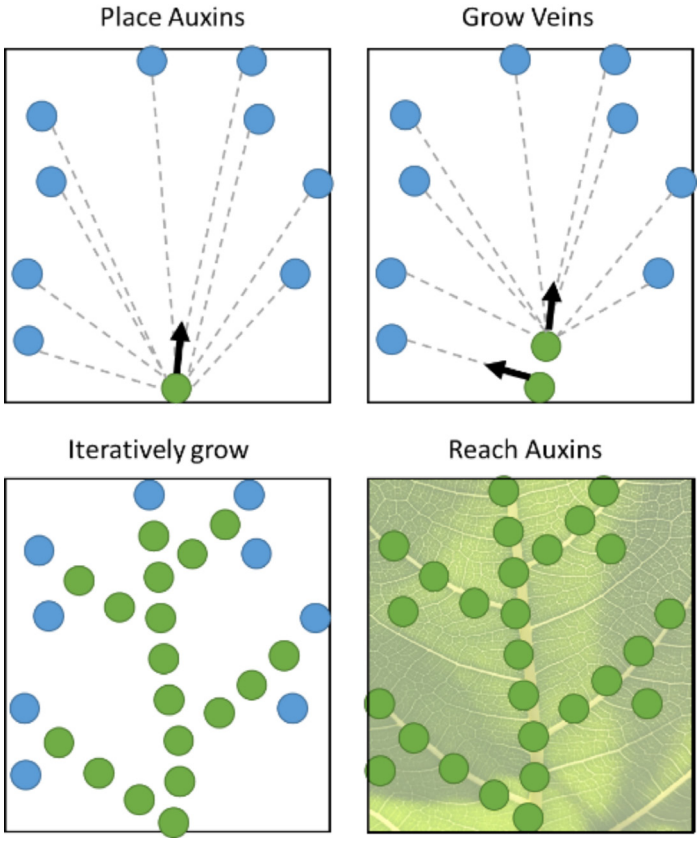


Figure 2. Sketch of the space colonization algorithm. Blue nodes represent growth hormone sources (auxins) and green nodes represent vein nodes. Vein nodes grow in the average direction of their nearest paired auxins.

This generative algorithm was coupled with a heat conduction finite element simulation to determine the temperature distribution of the domain for the source-to-sink problem shown in *Fig. 3*. The design domain, Ω, uniformly generates heat, which can be extracted from a fixed temperature boundary, Γ_D. The remaining boundaries, Γ_N, are adiabatic and restrict heat flow within the domain. The goal of this optimization problem is to distribute thermally conductive material on the domain, Ω, to reduce the average temperature on the domain, given a limited budget of conductive material. A genetic algorithm was used to adjust the tuning parameters of the generative algorithm for the optimization routine.

The optimization results obtained using the interaction-based method were compared with a voxel-based algorithm for a simple heat conduction problem given 100 total thermal simulations; refer to *Fig. 3*. The voxel-based method generated a tree-structure with no prior assumption on form but spent a significant portion of time (50+ iterations) refining a more defined structure. The design obtained with the voxel-based method has a peak temperature of 445°C on the domain. The interaction-based generative algorithm, optimized using a genetic algorithm, searches a diverse set of branching structures to identify several well-performing designs. Of the 100 designs tested using the interaction-based algorithm, several dozen featured lower temperatures on the domain

compared to the voxel-based design. The best design obtained using the interaction-based method has a maximum temperature of 292°C on the domain, which is a 34% improvement over the design obtained using the voxel-based method. Though both methods successfully produce designs that reduce the temperature of the domain, this example demonstrates how an improved search can be achieved when restricting the search space to a target class of structures. Carefully choosing an appropriate generative algorithm to represent a set target class of structures is one key to unlocking further improvements. The reader is referred to [1] for further details.

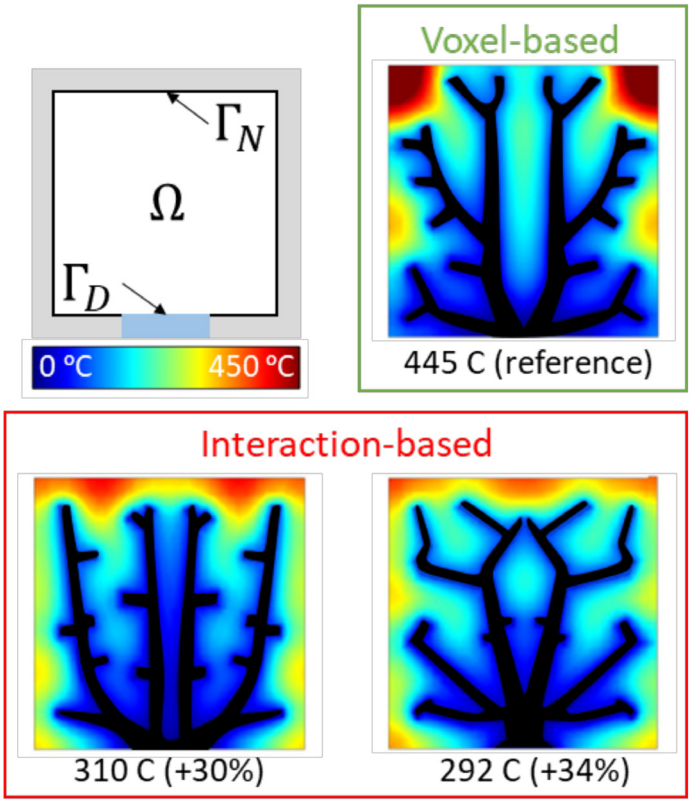


Figure 3. Source-to-sink thermal conductor design problem and results. The design domain and boundary conditions (top-left). A comparison of generated heat source-to-sink thermal conductor tree-structures between voxel-based (top-right) and interaction-based (bottom) optimization methods. Percentage improvement in maximum temperature from the reference is shown in parenthesis.

EXTENSIONS OF GENERATIVE DESIGN FOR ELECTRONICS COOLING

Generative design has been employed in a variety of applications related to electronics cooling. The design of thermal conductors by topology optimization has been explored relative to cooling an integrated circuit (IC) device in a power control unit [8]. Here, a designed prototype thermal conductor, *Fig. 4a*, was experimentally shown to provide reductions in the IC device maximum temperature of up to 60 °C. Optimization of thermal conductors has been extended to include design-dependent loads in the form of conformal heat transfer coefficient boundary conditions with application to additively manufactured air-cooled heat sinks for electronics [9]. In this case, an optimized, fabricated, and experimentally tested pin fin heat sink structure, *Fig. 4b*, demonstrated the highest coefficient of performance when compared with similar surface area plate and pin fin heat sink layouts reported in the literature.

The consideration of fluid flow for conjugate heat transfer further enriches the generative design of heat sinks or cold plates for electronics cooling. This field has grown rapidly since the first work on topology optimization for thermal-fluid systems [10, 11]. The method has been successfully applied using a local-global (unit cell-manifold) design approach for liquid-cooled cold plates for power electronics [12]; refer to *Fig. 4c*. Interesting further applications include the design of heat sinks subject to natural convection for light emitting diode (LED) lamps [3], the design of manifold microchannel heat sinks for power electronics [13], and three-dimensional design of heat exchangers relevant to system-level electronics cooling solutions [14], to name just a few.

A somewhat distinct application of generative design for electronics cooling pertains to the optimization of thermal composites or thermal metamaterials. Here, the anisotropic material thermal conductivity of thermal composites in various forms may be exploited to route heat, *Fig. 4d*, and protect temperature-sensitive components from heat-generating devices [15, 16]. Interestingly, the same anisotropic thermal composite technology may also be leveraged in the scavenging or harvesting of waste heat [17].

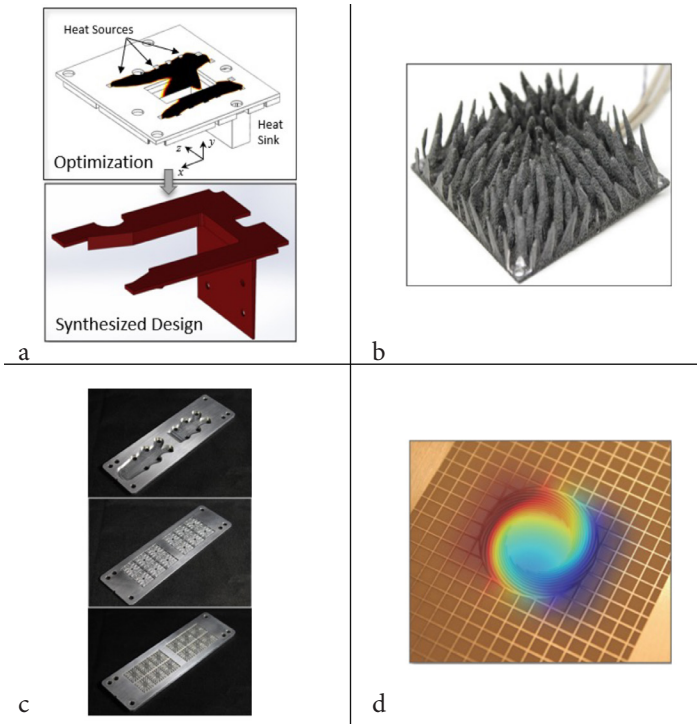


Figure 4. Example generative designs for electronics cooling: (a) thermal conductor for IC cooling; (b) heat sink for air cooling of electronics; (c) layers of a multi-pass branching microchannel cold plate for power electronics; (d) anisotropic thermal metamaterial printed-circuit board.

CONCLUSION

This article introduced the concept of generative design as it relates to practical engineering for electronics cooling. To review, generative design is an iterative process where a program is used to create a set of designs that meet product requirements. This can be achieved using a design abstraction to enable the efficient creation and search of optimal structures. The increased capability of modern computing, coupled with advances in materials and manufacturing, have enabled generative design to become practical today.

A demonstrative example of using generative algorithms to design biologically inspired branching thermal conductors was outlined to articulate how such a process can be realized. This included identifying a target class of structures to search, choosing an appropriate generative algorithm to create the desired structure, and using physics-based simulation in an optimization routine to identify the best design. It was observed that choosing an appropriate generative algorithm provides an improved selection of optimal structures and motivates careful consideration of generative methods for a design task.

In addition to this case study, several examples of using generative design for electronics cooling were discussed. This included the design of thermal conductors in a power control unit and air-cooled heat sink, various conjugate heat transfer problems for liquid cold plates and heat exchangers, and metamaterial design for thermal insulation and energy harvesting applications. These examples represent a subset of ways generative design is being used today to enhance electronics cooling.

REFERENCES:

[1] D. J. Lohan, E.M. Dede, and J.T. Allison, Topology optimization for heat conduction using generative design algorithms. Structural and Multidisciplinary Optimization, 55, pp. 1063-1077 (2017).

[2] E. M. Dede and Y. Liu, Experimental and numerical investigation of a multi-pass branching microchannel heat sink. Applied Thermal Engineering, 55(1-2), pp. 51-60 (2013).

[3] J. Alexandersen, O. Sigmund, K. E. Meyer, and B. S. Lazarov, Design of passive coolers for light-emitting diode lamps using topology optimization. International Journal of Heat and Mass Transfer, 122, pp. 138-149 (2018).

[4] A. Bejan and S. Lorente, Constructal theory of generation of configuration in nature and engineering. Journal of Applied Physics, 100(4), p. 041301 (2006).

[5] A. Runions, B. Lane, and P. Prusinkiewicz, Modeling trees with a space colonization algorithm. In: Eurographics workshop on national phenomena, pp. 63–70 (2007).

[6] M. P. Bendsoe and O. Sigmund, Topology optimization - theory, methods, and application, 2nd edn. Springer (2004).

[7] T. Sachs, The control of the patterned differentiation of vascular tissues. Advances in Botanical Research, 9, pp. 151-262 (1981).

[8] E. M. Dede, Y. Liu, S. N. Joshi, F. Zhou, D. J. Lohan, and J. Shin, Optimal design of three-dimensional heat flow structures for power electronics applications. ASME Journal of Thermal Science and Engineering Applications, 11(2), 021011 (2019).

[9] E. M. Dede, S. N. Joshi, and F. Zhou, Topology optimization, additive layer manufacturing, and experimental testing of an air-cooled heat sink. ASME Journal of Mechanical Design, 137(11), 111403 (2015).

[10] E. M. Dede, Multiphysics topology optimization of heat transfer and fluid flow systems. In: COMSOL Conference Boston, pp. 1-7 (2009).

[11] G. H. Yoon, Topological design of heat dissipating structure with forced convective heat transfer. Journal Mechanical Science and Technology, 24(6), pp. 1225-1233 (2010).

[12] E. M. Dede, Single-phase microchannel cold plate for hybrid vehicle electronics. In: Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), pp. 118-124 (2014).

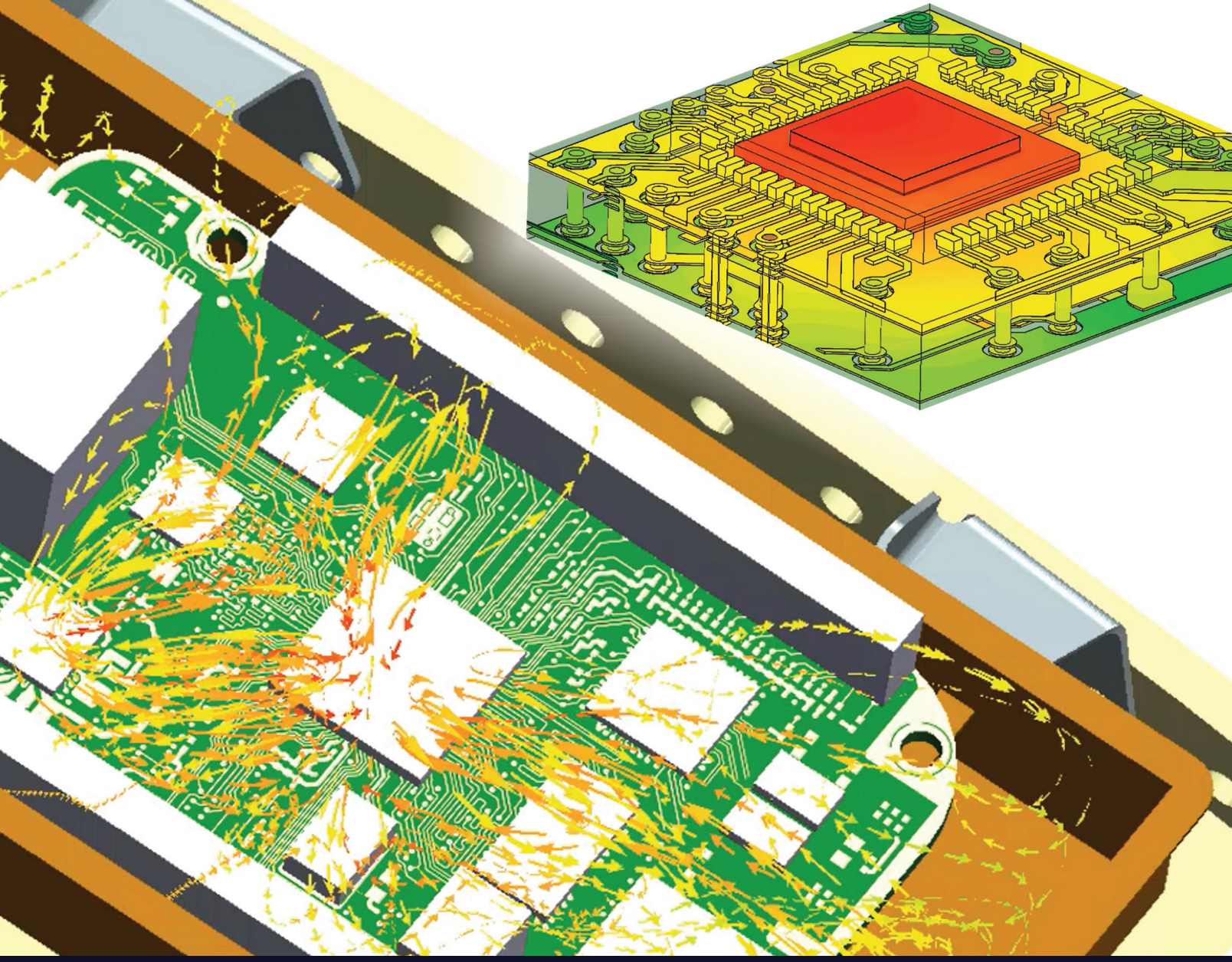
[13] Y. Zhou, T. Nomura, and E. M. Dede, Topology optimization of manifold microchannel heat sinks. In: 19th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), pp. 740-746 (2020).

[14] F. Feppon, G. Allaire, C. Dapogny, and P. Jolivet, Body-fitted topology optimization of 2D and 3D fluid-to-fluid heat exchangers. Computer Methods in Applied Mechanics and Engineering, 376, p. 113638 (2021).

[15] E. M. Dede, P. Schmalenberg, T. Nomura and M. Ishigaki, Design of anisotropic thermal conductivity in multilayer printed circuit boards. IEEE Transactions on Components, Packaging and Manufacturing Technology, 5(12), pp. 1763-1774 (2015).

[16] J. C. Kim, Z. Ren, A. Yuksel, E. M. Dede, P. R. Bandaru, D. Oh, and J. Lee, Recent advances in thermal metamaterials and their future applications for electronics packaging. ASME Journal of Electronic Packaging, 143(1), p. 010801 (2021).

[17] E. M. Dede, P. Schmalenberg, C.-M. Wang, F. Zhou, and T. Nomura, Collection of low-grade waste heat for enhanced energy harvesting. AIP Advances, 6, p. 055113 (2016)



Enhance thermo-mechanical analysis workflows

Leverage efficient CFD to FEA worfklows for shorter, robust thermal and thermo-mechanical stress analysis. Discover how to create 3D transient temperature field results in CFD and map to an FEA mesh easily.

Simcenter portfolio includes leading electronics cooling software, CAD-embedded analysis, and multi-physics analysis tools to support a wider range of user skill and experience demographic from analyst to designer.

www.siemens.com/simcenter

SIEMENS

A Heatsink Remodelling Methodology

Robin Bornoff, PhD
Siemens Digital Industry Software

The role of a heatsink is to provide a conduction path from a heat source that is to be cooled to a volume of cooling fluid. The heatsink's surface area that fills that volume is considerably larger than the surface area of the heat source. In this way, the heatsink acts as an 'area extender'.

$$T_{source} = \left(\frac{Q}{hA}\right) + T_{ambient} \quad (1)$$

For a given heat flow (Q) and convective heat transfer coefficient (h), any increase in the surface area will result in a decrease in the temperature rise of the source over ambient (*Equation 1*).

Filling a design volume with a shape with a large surface area has its drawbacks, however. If the surface area is too large the fluid flow channels through it will be very narrow. This can result in thermal choking where the fluid temperature attains a similar temperature to the heatsink surface and thus little heat transfer is achieved. In addition, any fluid approaching the heatsink will be more likely to divert around it or, for a ducted heatsink, a bigger fan or pump is required to force the fluid through it. With too little surface area, the fluid would readily pass through the heatsink, wouldn't thermally choke, but with less surface area than optimal, the thermal performance would be compromised.

It is this trade-off that makes heatsink design so well suited for optimization. The topologies of classic heatsinks are parametrically defined, due primarily to manufacturing constraints that require extrudable or millable shapes. Be they pin fin or plate, a small number of parameters defines (and constrains) the shape, e.g., base thickness, width, length, number of fins/pins, etc. Various optimization strategies can be applied to minimize some objective cost function (e.g. maximum heatsink temperature) to identify the corresponding set of optimal parameters. However, the resulting topology will always be the same.

GENERATIVE DESIGN

The advent of additive manufacturing methods has led to the question 'if most manufacturing constraints are removed, how can simulation be applied to identify an optimal geometry?'. Generative Design applies simulation techniques to identify an optimal geometry without being constrained by parametric assumptions. The most common approach is to perform a standard simulation on a given model (a primal solution), then perform an adjoint solution that predicts the resultant sensitivities of that model to local changes made to it. Those small adjoint recommended changes are made and the process is repeated until such time as the model converges to an optimum state. Typical resulting geometries are often very 'organic' in nature and far from parameterisable.

THERMAL BOTTLENECK DRIVEN TOPOLOGY IDENTIFICATION

Instead of having to perform an adjoint solution at each stage of the iterative process, is there a way in which just the primal solution might be used to identify where small beneficial incremental changes to the model might be made? The Thermal Bottleneck parameter [1] is intended to identify areas of a thermal model through which heat flows AND in which heat is finding it difficult

Robin Bornoff, PhD
After receiving a bachelor's degree in Mechanical Engineering in 1992 and a PhD for CFD research in 1996 from Brunel University in the UK, Robin joined Flomerics as a Flotherm support and application engineer. By the time of the acquisition of Flomerics by Mentor Graphics in 2008 he was the Product Marketing Manager for Flotherm. Now in Siemens Digital Industry Software, he is a Senior Key Expert in the Simulation and Test Solution division. With over 25 years' experience in the field of electronics thermal simulation, he has published over 30 journal and conference papers and has had 7 patents granted

to flow. It is defined as the dot product of the heat flux vector and temperature gradient vector at any given point.

For heatsink applications, areas where the Thermal Bottleneck is large on the periphery of the geometry indicate regions that might benefit from being 'relieved' by a local area extension (e.g., a bit of heatsink geometry is added there). Conversely, where the Thermal Bottleneck is low on the periphery indicates areas that are much less critical and so might be removed. The heatsink is modified at those locations (bit added, bit removed), a new primal simulation is performed and the process is repeated until a nominated cost function no longer decreases, i.e., no subsequent change will improve performance. In this way, any given heatsink geometry can be 'remodeled' so as to seek an improved performance.

The Thermal Bottleneck parameter is a leading indicator of regions where the heatsink geometry might be locally adjusted by adding and removing small parts of the geometry. However, there is no absolute guarantee that making these small modifications at those locations will be beneficial. Therefore the process entails performing 3 individual (parallel) simulations; a bit added, a bit removed and both a bit added and a bit removed. The cost function for each can be observed and the best one is chosen as a base for the next stage in the iterative process.

By way of an example to demonstrate this process, *Figure 1* shows a quarter model of a circular base pin fin heatsink.

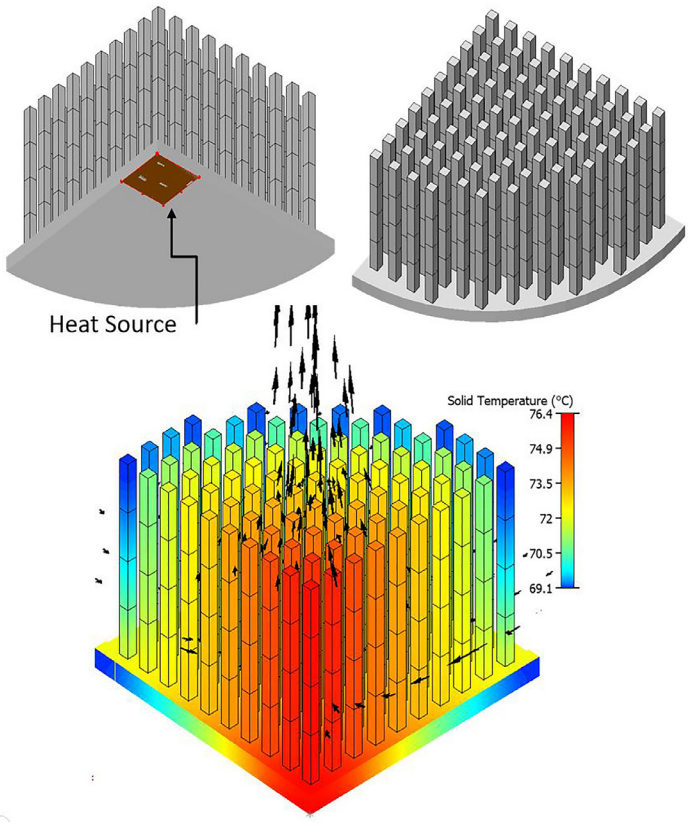


Figure 1 Quarter Model Pin Fin Heatsink Cooled Under Natural Convection

The heatsink cools a small centrally located heat source on the bottom of the base by natural convection. A full conjugate 3D CFD thermal simulation is conducted with 2 symmetry planes defined to represent the other 3 quarters of the heatsink. As expected, the central pins above the heat source are the hottest. Each of the pins is discretised into small rod elements. It is these small bodies that will either be removed or an identical part added to.

For this simple example, the addition and subtraction of bodies are constrained such that only the Thermal Bottleneck in the top tip bodies of each pin is considered. In this way, remodeling the heatsink only changes the height of each pin being varied: a 1D type remodeling.

The cost function is taken as the maximum heatsink temperature. This occurs at a location directly above the heat source and is directly proportional to the overall thermal resistance.

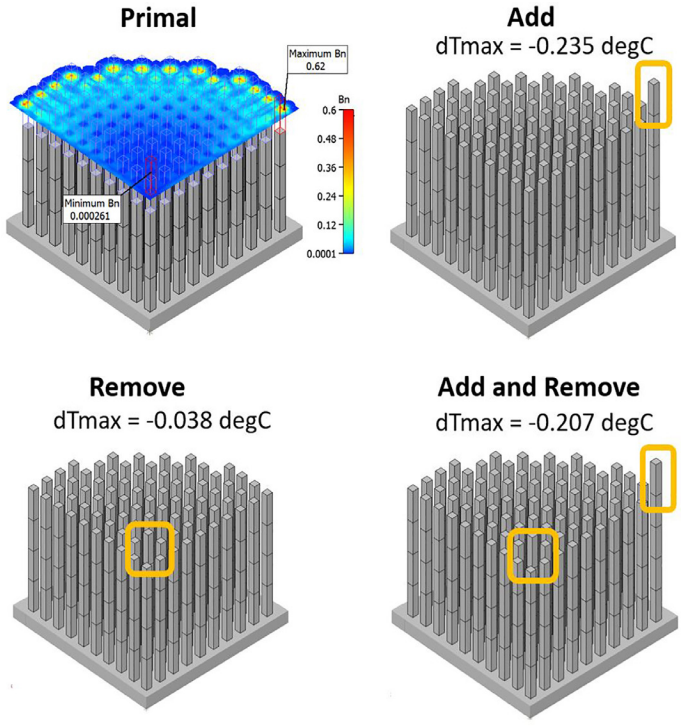


Figure 2 First Stage of the Remodeling Process

The first step in the remodeling process is shown in *Figure 2*. Despite the central pins being the hottest, their tips have the lowest Thermal Bottleneck. The highest Thermal Bottleneck is located on the tip of a peripheral pin. Three resulting models are simulated: one with a body added to the pin tip with the highest Thermal Bottleneck, a second one in which the body is removed from the pin tip with the lowest Thermal Bottleneck and, in the third, both an addition and a subtraction are made. All three decrease the temperature rise of the heatsink, but it is the addition case that leads to the biggest decrease in temperature rise. This, therefore, forms the base model of the next stage of an iterative process.

The process is then repeated until such time as no subsequent modifications result in a temperature rise decrease.

1D REMODELING EXAMPLE

Using the same application as above, an initial heatsink to be remodeled has each pin defined at a random height from zero to a maximum design space height. This test was performed as part of an investigation into the sensitivity of the initial heatsink geometry to the final optimized state.

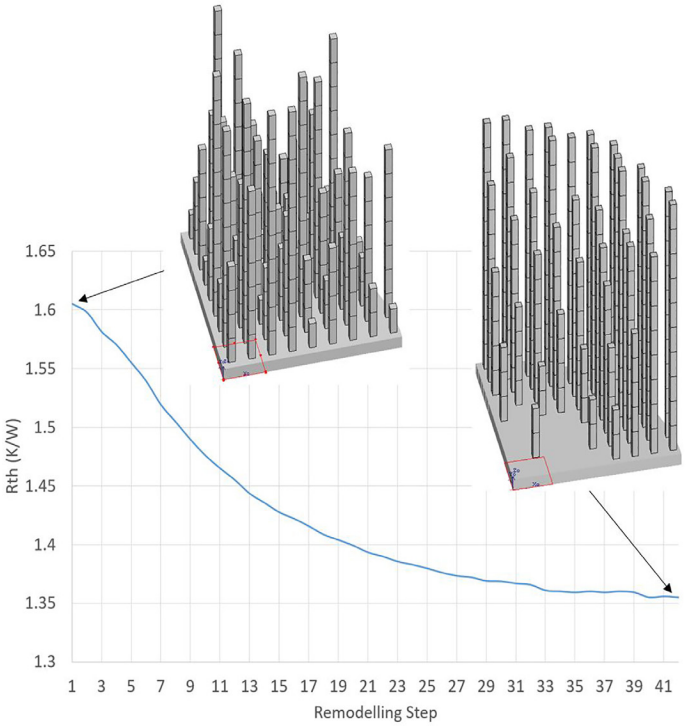


Figure 3 1D Constrained Heatsink Remodeling

The optimal design (which was proven independent of the initial heatsink geometry) has the peripheral pins at a maximum design space height whilst the central pins above the heat source are all but removed. The heights of the pins increase between the center and the periphery.

The periphery of the heatsink has a larger area exposed to ambient, so the pin surface area benefits from maximizing there. It is much more difficult for the cool ambient air to penetrate into the central congested area of the heatsink, thus making the pins there redundant and leading to their being removed by the remodeling.

It could be argued that such a simple and constrained example could be parametrically defined (i.e. pin height) and optimized using more standard approaches. In this example, there are 60 pins and so there would be 60 degrees of freedom for the optimizer to consider. The Thermal Bottleneck-driven remodeling process identifies an optimum in only 41 steps using a physics-based approach as opposed to a purely numerical one.

2D REMODELING EXAMPLE

By controlling the discretisation of a heatsink geometry, extrudable, or at least prismatic geometries can be realized. Consider a standard plate fin extrusion. By discretising it into tessellated bodies that are the full (extruded) length of the heatsink, and only allowing for these full-length bodies to be removed or added to with similarly shaped full-length bodies, a resulting 2D profile can be maintained.

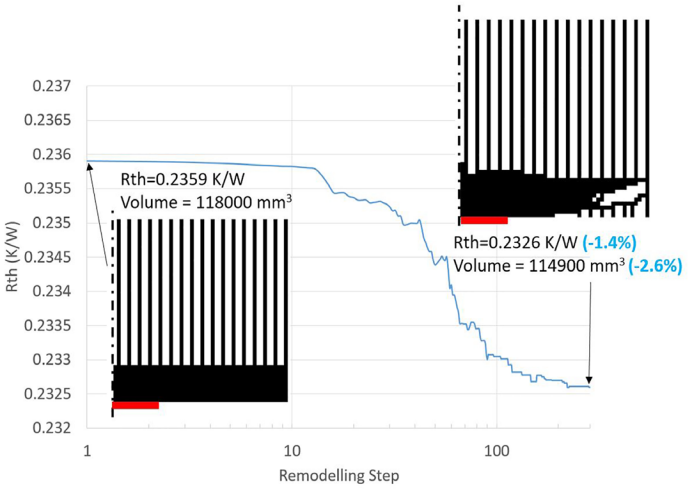


Figure 4 2D Constrained Heatsink Remodeling

Figure 4 shows the remodeling process applied to the plate fin parametrically-defined heatsink. Again, symmetry is employed so as to only model half of the geometry. The heat source is centrally located on the base (red line in *Figure 4*). The heatsink is subjected to forced convection air cooling. The original heatsink is discretised into square section, full-length rods of the same dimension as the fin width.

The remodeling process results in a small improvement both in terms of thermal resistance and volume (mass). Specifically, additional surface area is achieved by carving out flow channels in the base, on the periphery away from the central heat source. The base does not need to be as thick in this region as it has less heat to spread. Removing some of its geometry so as to create new flow channels both reduces the mass and increases heat transfer area. It is noted that, despite their parametric simplicity, forced convection plate fin heatsinks are already surprisingly effective.

3D REMODELING EXAMPLE

A heat sink can be discretised into a 3D collection of tessellated bodies such that for any location of the biggest Thermal Bottleneck body, a same-sized cuboidal body might be added to any of its air apparent faces. Similarly, any body might be removed allowing for holes to appear. For this example, a half model of a vertically oriented natural convection cooled heatsink is considered (*Figure 5*).

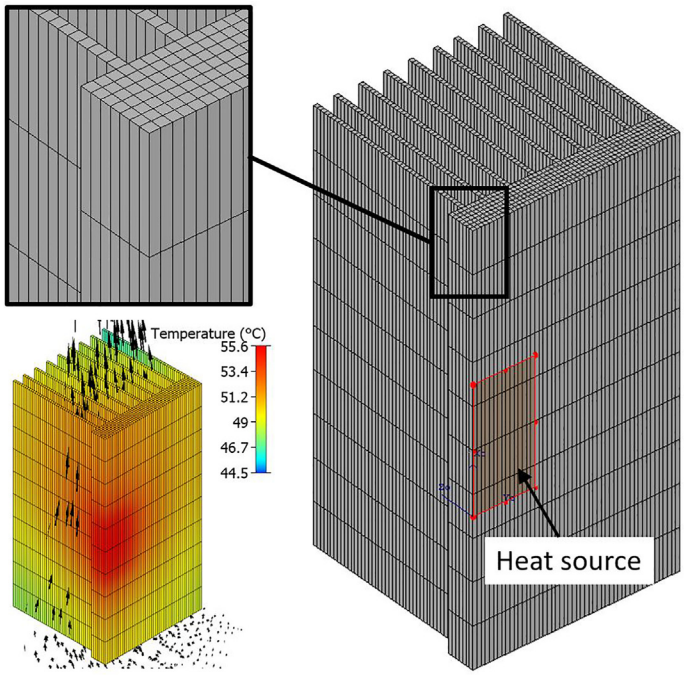


Figure 5 3D Discretised Natural Convection Half Model Heatsink

With a larger number of bodies comes a greater flexibility for novel topologies to emerge during the remodeling process. This, however, comes hand in hand with prolonged remodeling simulation times as many more steps are possible until an optimal design is identified.

4.6% reduction in thermal resistance (1.41 to 1.34 K/W)
18% reduction in volume (73700 to 60660 mm^3)
1.4% reduction in surface area (90274 to 89018 mm^2)

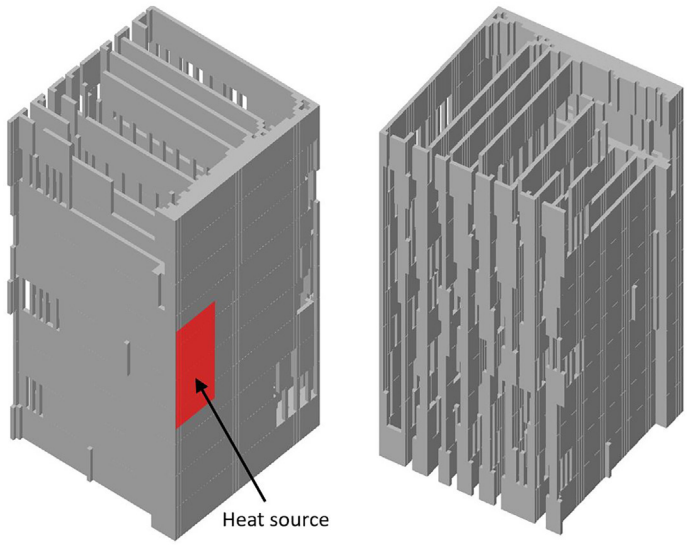


Figure 6 End Result of the 3D Remodeling Process

The resulting optimized heatsink generated by remodeling in 3 dimensions is shown in *Figure 6*. Whereas a modest 4.6% reduction in thermal resistance was seen, a more significant reduction in volume (mass) of 18% was achieved. There was only a 1.4% reduction in surface area though. In this case, the remodeling achieved a redistribution of extended surface area, bespoke to the cooling environment. The surface area at the downstream (top) part of the heatsink was redistributed to plates connecting to the tops of the fins. Also, the base at the top of the heatsink was carved out, with less effect on surface area but a greater effect on minimizing mass. It is also interesting to note the 'frame' type geometry that emerges with equally spaces gaps in some areas of the fins.

While the bottom part of the heatsink is most efficient, as that is where the cooling ambient air enters, the top part is less efficient due to the preheating of the air as it passes up through the heatsink and so substantial remodeling occurred there.

Although the resulting geometry proved to be more efficient than the original design, the somewhat coarse discretisation results in a stepped geometry. A more refined geometry would be generated by the remodeling process if the size of the discretised bodies had been smaller. It is envisioned that a post-processing smoothing stage would be applied to further refine the heatsink geometry in a similar manner to what is required to smooth out any numerical artifacts of some adjoint-based topology optimizations. This would be done in addition to any other required changes identified by additive manufacture validation checks.

CONCLUSION

The opportunities that additive manufacturing provides have necessitated the new approach of 'Generative Design'. Unconstrained by parametric topologies, and not reliant on legacy engineering expertise, approaches such as adjoint-based Topology Optimization and the remodeling method presented here will gain traction as additive manufacturing itself matures and becomes more cost effective.

REFERENCES

[1] R. Bornoff, B. Blackmore and J. Parry, "Heat sink design optimization using the thermal bottleneck concept," 2011 27th Annual IEEE Semiconductor Thermal Measurement and Management Symposium, San Jose, CA, 2011, pp. 76-80, doi: 10.1109/STHERM.2011.5767181.

Thermal Modeling of a Silicon Germanium (SiGe) Radio Frequency Integrated Circuit (RFIC) for Wireless Communications

Todd Salamon
Nokia Bell Labs, Hybrid Integration Research Group

The creation, transport and storage of digital information are growing at rates of 40% to 50% annually, with video, mobile broadband, and machine-to-machine communication being the main drivers. The implementation of 5G wireless networks is enabling this growth and heralding a new era of revolutionary applications and functionality due to bandwidth increases and communication latency reductions. Key 5G network enablers include new frequency spectrum (e.g., mmWave), massive multiple-input/multiple-output (MIMO) technology and new material systems. Silicon germanium (SiGe) is one material system that offers the potential to develop Radio Frequency Integrated Circuit (RFIC) technology integrating many analog functions into a single integrated circuit, thereby realizing significant reductions in system size, with concomitant cost and power savings.

In this article, we present a methodology for simulating die-level heat transfer for an RFIC comprising SiGe devices on a flip-chipped silicon die. This is a challenging thermal problem as the RFIC form factor has shrunk by over two orders of magnitude relative to its analog counterpart, leading to a proportional (100X) increase in heat density that makes package-level thermal management challenging. *Fig. 1* (right) shows a photograph of the die studied in this work, which is a transceiver designed for the 27-43.5 GHz frequency range [1]. The goal of the modeling work is to characterize the thermal behavior of the SiGe RFIC to optimize the thermal design and ensure that the device does not exceed the manufacturer-specified Safe Operating Area (SOA) during its lifetime.

THERMAL MODELING

SiGe transistor junction temperature modeling

Fig. 1 (right) shows a schematic cross-section of a SiGe heterojunction bipolar transistor. Modeling the thermal behavior of this transistor using a first-principles, physics-based approach is challenging as it requires precise information about material properties and geometry of the structures comprising the transistor, and which may be considered proprietary and confidential by a foundry.

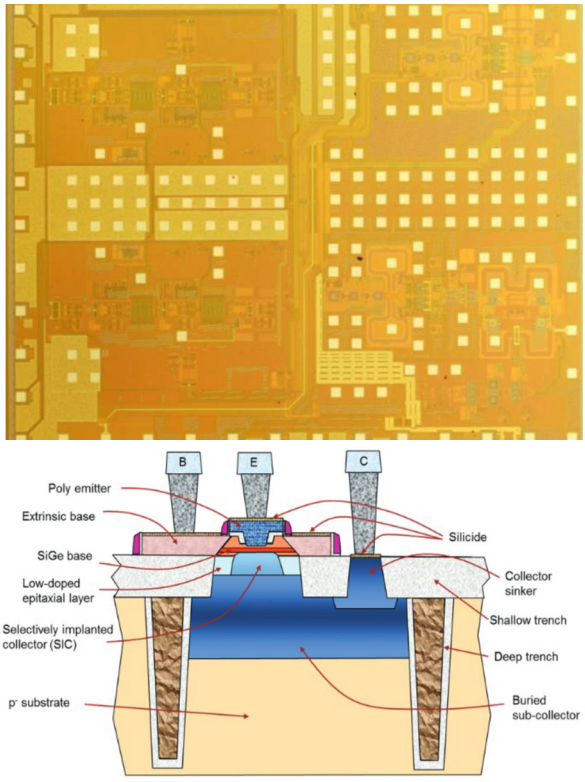


Figure 1: (top) Die photograph of the 27-43.5 GHz transceiver [1] studied as part of this work; and (bottom) Schematic of a cross section of a SiGe heterojunction bipolar transistor (HBT) [2]

Todd R. Salamon
Todd received the Ph.D. degree in chemical engineering from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA. He is currently a Member of Technical Staff in the Hybrid Integration Research Group, Nokia Bell Labs, Murray Hill, NJ, USA, where he has worked on thermal management, microfluidics, transport phenomena in optical fiber manufacturing, and Raman and erbium amplifier dynamics and control in transparent optical networks. He has authored over 60 publications and conference presentations and holds 36 issued or pending patents. He was the Principal Investigator on a U.S. Department of Energy project to develop and commercialize refrigerant-based cooling technology targeting the Information and Communications Technology (ICT) sector, and a Team Member of the MIT-led DARPA ICECool Fundamentals Program.

In this work, we utilize an alternative approach based on empirical characterization of individual transistors fabricated by the foundry, where the transistor junction temperature (T_j) can be represented by the following formula

$$T_j = T_{loc} + R_{th,loc}(T_{loc}) \times P_{device} \quad (1)$$

$$R_{th,loc}(T_{loc}) = A \times exp[B \times (T_{loc} - T_{ref})] \quad (2)$$

where T_{loc} is the local silicon die temperature, $R_{th,loc}(T_{loc})$ is the thermal resistance of the transistor, P_{device} is the transistor power, A and B are empirical constants determined from experimental characterization of the device, and T_{ref} is a reference temperature [3].

Structure	Material	Thermal resistance [C/W]	% of total thermal resistance
Leadframe	Copper	38.9	16.0%
Copper pillar bump	solder	105.8	43.6%
	barrier	4.6	1.9%
	Cu bump	20.9	8.6%
	Cu opening	6.5	2.7%
	UBM	2.4	1.0%
Pad	Metal N	63.6	26.2%
	Via N-1		
	Metal N-1		
	…		
	Via1		
	Metal 1		
	contact		
Total		242.9	100%

Table 1: Thermal resistance values and relative percentage of the total thermal resistance stack for the leadframe, copper pillar bump and pad as predicted by Eqs. (5) and (6).

Eqs. (1) and *(2)* provide junction temperature information for low values of P_{device}, where self-heating effects are small. To account for device self-heating, which can result in large local changes in material thermal conductivities, we utilize the model of Paaschens *et al.* [3], which assumes the device thermal conductivity has the following temperature dependence

$$k = k_{ref}\left(\frac{T_{ref}}{T}\right)^{\alpha}, \quad (3)$$

resulting in the following equation for T_j

$$T_j = T_{loc} + R_{th} \times P_{device}, \quad (4)$$

where

$$R_{th} = T_{loc}\frac{\left[\left(1+\frac{(1-\alpha)P_{device}R_{th,loc}(T_{loc})}{T_{loc}}\right)^{\frac{1}{1-\alpha}} - 1\right]}{P_{device}},$$

k_{ref} is the local thermal conductivity of the device at a reference temperature T_{ref}, α characterizes the decrease of the device thermal conductivity with temperature, and $R_{th,loc}(T_{loc})$ is given by *Eq. (2)*.

SOLDER BUMP, CONTACT PAD AND LEADFRAME THERMAL RESISTANCE

The flip-chipped silicon die studied in this work is attached to the leadframe using copper pillar bumps [4][5]. In addition to providing signal and ground connections, the copper pillar bumps are the primary path for transferring the dissipated power from the SiGe transistors. In particular, the layout includes a dedicated subset of "thermal" bumps whose role is for heat transport.

The simplest approach to modeling the layers within the copper pillar bump, pad and leadframe is as thermal resistances in series, e.g.,

$$R_i = \frac{h_i}{A_i k_i},$$

where h_i, A_i, and k_i are the thickness, area, and thermal conductivity of the individual layers. The series resistance approach predicts a total thermal resistance from the pad to the lead frame of 242.9 C/W, with the individual contributions to the total thermal resistance being 26.2%, 57.8% and 16.0%, respectively, for the pad, copper pillar bump and leadframe (see *Table 1*).

To account for spreading and constriction resistance effects not captured in the series resistance approach, a detailed numerical model was constructed with commercially available software [6]. The computed temperature field is shown in *Fig. 2* (next page). This structure has a thermal resistance of

$$R^{\text{numerical}}_{\text{leadframe+bump+pad}} = 280\frac{\text{C}}{\text{W}},$$

which is approximately 15% larger than the analytical formula, indicating that the analytical series resistance approach is reasonable while the detailed numerical model provides additional accuracy. We also note that the numerical model can be readily extended to account for important effects such as solder wetting; see, for example, *Fig. 2* (next page).

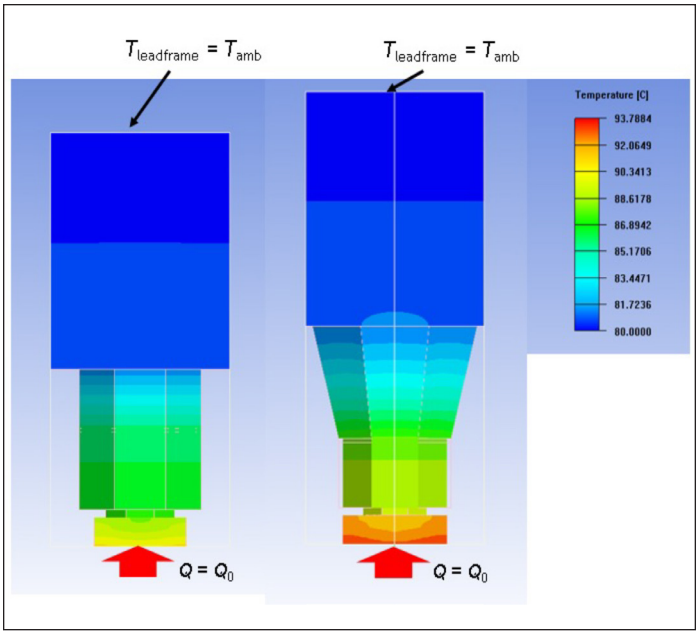


Figure 2: Temperature contours for structures comprising a contact pad, copper pillar bump and leadframe: (left) untapered solder region with $R^{numerical}_{leadframe+bump+pad}$ = 280 C/W; and (right) tapered solder region with $R^{numerical}_{leadframe+bump+pad}$ = 343 C/W.

DIE LEVEL THERMAL MODELING

Approximation to the detailed thermal bump model

The thermal bump numerical model comes at a computational cost, as the grid used to resolve the temperature field can comprise over 1 million nodes. A coarser grid may decrease the computational cost. However, as the application has several hundred thermal bumps, it is anticipated this approach would not scale well computationally. Instead, we replace the detailed model with an approximate boundary condition where the pad interfaces with the silicon substrate

$$-k_{Si}\left.\frac{dT_{Si}}{dn}\right|_{\partial D_{pad}} = \frac{1}{R_{bump}A_{pad}} \times \left(T_{Si} - T_{amb}\right)\Big|_{\partial D_{pad}} \quad (5)$$

where the left hand side term corresponds to the silicon conductive heat flux, $R_{bump} \equiv R^{numerical}_{leadframe+bump+pad}$ is the thermal resistance of the thermal bump as calculated from the detailed computational model, and A_{pad} is the pad area in contact with the silicon substrate.

Fig. 3 shows a comparison of the detailed and approximate boundary condition models. The similar silicon die temperature contours indicate the approximate boundary condition is a reasonable proxy for the detailed numerical model, while the grid size decreased from ~610k nodes in the detailed model to ~91k nodes in the approximate model - a significant computational cost reduction. Simulations show that, for a range of bump to heat source distances, the relative error in the heat source to leadframe thermal resistance is below 2.5%, which is an acceptable trade-off to realize a computationally tractable die-level thermal model, which we discuss in the following section.

Die level thermal modeling – spread heat source approach

A spread heat source model is constructed by dividing the transistors and supporting devices into 14 groupings, with each grouping G_i assumed to dissipate its power uniformly over the area occupied by that functional block. *Fig. 4* (next page) shows the silicon die with the 14 transistor groupings, denoted by the green polygons, with a total heat dissipation of 4.65 Watts. Heat transfer to the lead frame is facilitated by 150+ thermal bumps, denoted by the white squares, while conduction through underfill is accounted for on the remainder of the die.

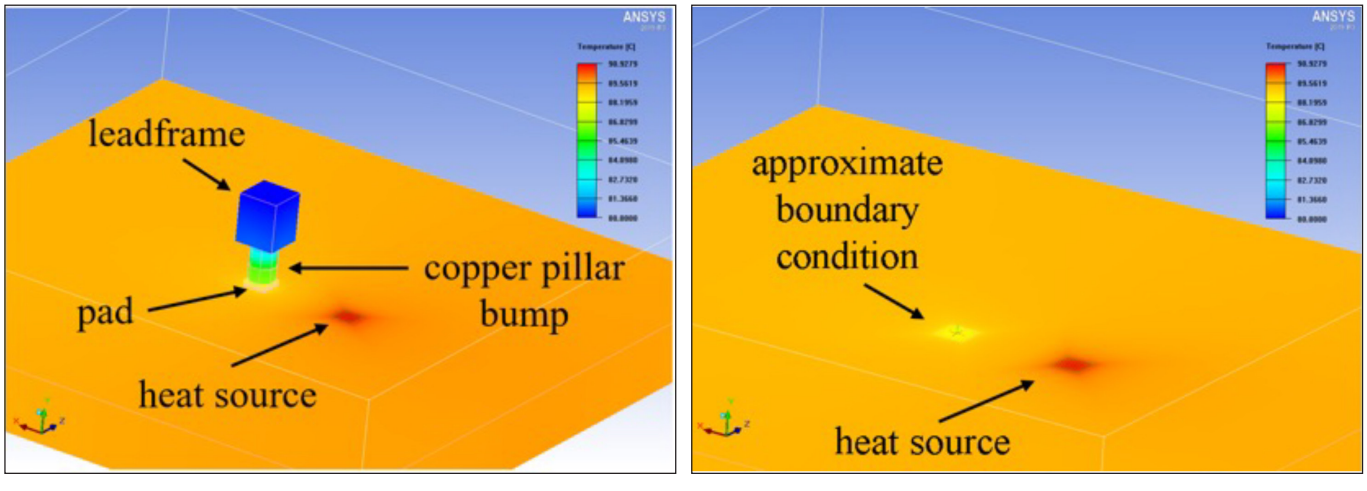


Figure 3: Computed temperature contours for numerical models for detailed (left) and approximate (right) thermal models for heat transfer through a thermal bump (pad+copper pillar bump) that is shifted 300 μm laterally from a 73μm x 73μm heat source dissipating 20 mW on a 200 μm thick silicon die. (color contour range: 80-90.9°C)

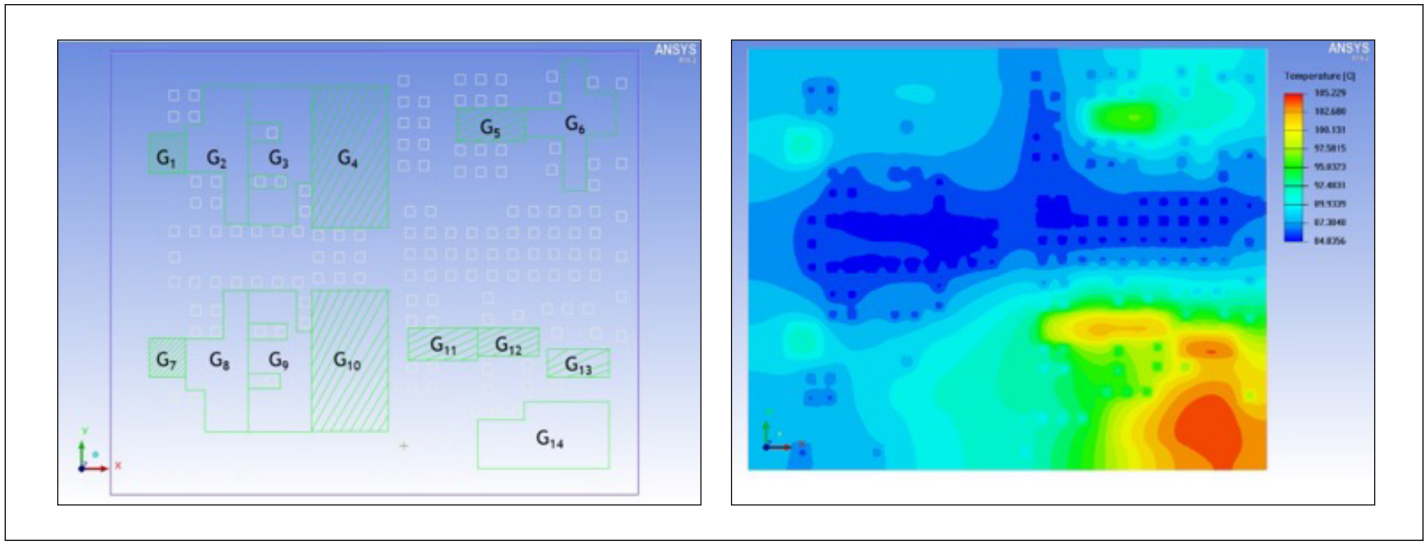


Figure 4: (left) Die level spread heat source thermal model consisting of 14 transistor groupings (green polygons) dissipating a total of 4.65 W and 150+ thermal bumps (white squares). The silicon die (purple rectangle) is approximately 4.1 mm (width) x 3.5 mm (height) x 0.2 mm (thickness); and (right) Temperature contours for the spread heat source thermal model presented in Fig. 4 (left). The maximum temperature rise of the silicon die is approximately 25.2°C above the lead frame temperature of 80°C. (color range : 84.8 – 105.2°C)

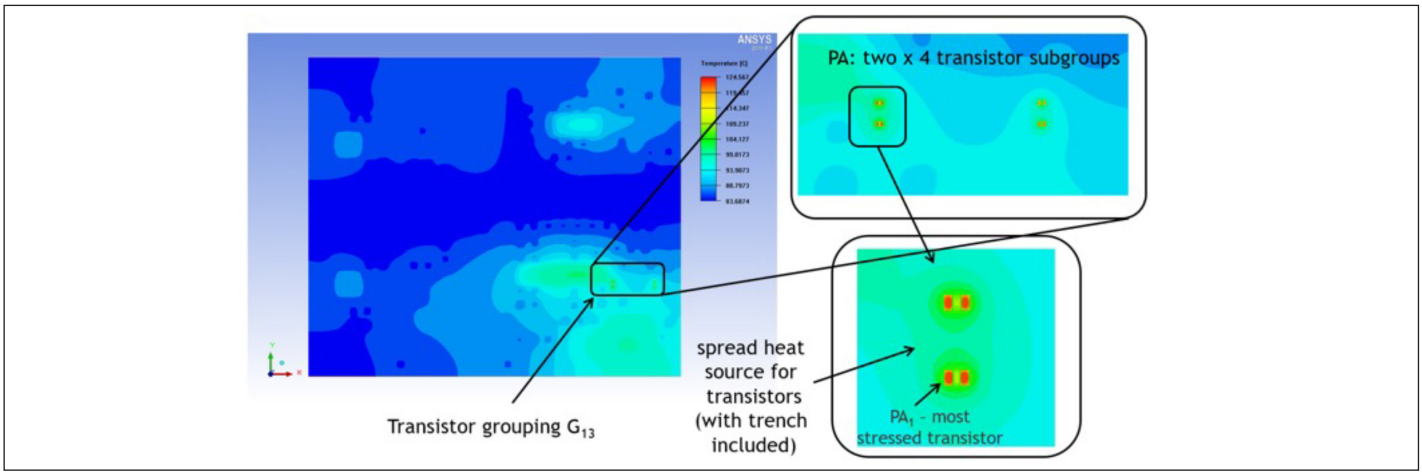


Figure 5: Temperature contours for the spread heat source model presented in Fig. 4 and incorporating a detailed model for transistor grouping G_{13}. *(color contour range: 83.7 – 124.6°C)*

Temperature contours across the silicon die are shown in *Fig. 4* (above) for the spread heat source model. The maximum die temperature rise is 25.2°C and occurs in the lower right-hand portion of the device. We note that this region contains 47% of the total heat dissipation (from transistor groupings G_{11} through G_{14}) and has a lower thermal bump density compared to the remainder of the silicon die. The silicon die temperature provides useful information for device designers, for example, to mitigate potential deleterious effects of electromigration, which are accelerated at elevated temperatures.

Most stressed SiGe transistor junction temperature estimation

The results shown in *Fig. 4*, coupled with knowledge of transistor power densities, indicate that the most stressed transistor is associated with grouping G_{13}, a power amplifier comprising 2 subgroupings of 4 identical transistors. A more representative model of grouping Q_{13} is constructed by assuming individual transistor power is dissipated uniformly within its footprint and incorporating confinement effects associated with the silicon dioxide/polysilicon deep trench surrounding each transistor. *Fig. 5* shows temperature contours for this detailed thermal model of transistor grouping G_{13}, with the remaining transistors groupings modeled using the spread heat source approach. We note that the silicon die maximum temperature is now significantly greater with the localization of transistor heat dissipation in grouping G_{13}; contrast T_{max} of ~124.6°C in *Fig. 5* with T_{max} of ~105.2°C in *Fig. 4*. The temperature contours shown in *Fig. 5* also indicate that transistor PA_1 has the highest temperature of the 8 transistors within the grouping G_{13}.

Estimating the junction temperature for transistor PA_1 using *Eqs. (3)* and *(4)* requires knowledge of the local silicon temperature near this device, namely $T_{loc,PA1}$, when this transistor is in the "off" state. This is calculated by assuming the following power distribution in grouping G_{13}

$$P_{PA1} = 0, P_{PA2} = P_{PA3} = \ldots = P_{PA8} = P_{const}.$$

$T_{loc,PA1}$ is plotted as a function of the normalized transistor power P_{const}/P_{max} in *Fig. 6* (next page), where P_{max} is the maximum anticipated transistor power.

Knowledge of the local silicon temperature for transistor PA_1 allows an estimation of its junction temperature using *Eqs. (3)* and *(4)*. *Fig. 6* (next page) shows the predicted junction temperature for transistor PA_1 as a function of the normalized transistor power and for various values of α. We note that the predicted junction temperature at $P_{const} = P_{max}$ (see inset table in *Fig. 6 next page*) ranges from 152.4°C for no temperature dependence ($\alpha = 0$) to 157.9°C for $\alpha = 1.333$, which is characteristic of bulk silicon, to 161.2°C for $\alpha = 2$, which is characteristic of foundry data. The predicted junction temperature provides useful information to assess the reliability of the device given potential usage scenarios and to ensure the device does not exceed the manufacturer-specified Safe Operating Area (SOA) during its lifetime.

In summary, this article has presented a modeling approach to characterize the thermal behavior of a SiGe RFIC for wireless communications. Key takeaways and lessons learned from this work include:

- 1D analytical models are useful for initial estimates of copper pillar bump and underfill thermal resistance.
- Detailed computational models are essential for quantifying spreading and constriction resistance effects at the thermal bump, silicon die and transistor footprint levels as well as quantifying thermal cross-talk between adjacent devices such as transistor groupings and individual transistors within a grouping.
- The compact model for heat transfer through the thermal bump is essential for reducing the computational complexity of the overall die-level thermal model with a minimal impact on accuracy.
- Incorporation of empirical foundry data for individual transistor thermal performance into the overall modeling framework allows for realistic estimates of device junction temperatures and obviates the need to construct a first-principles, physics-based model of a SiGe heterojunction bipolar transistor.

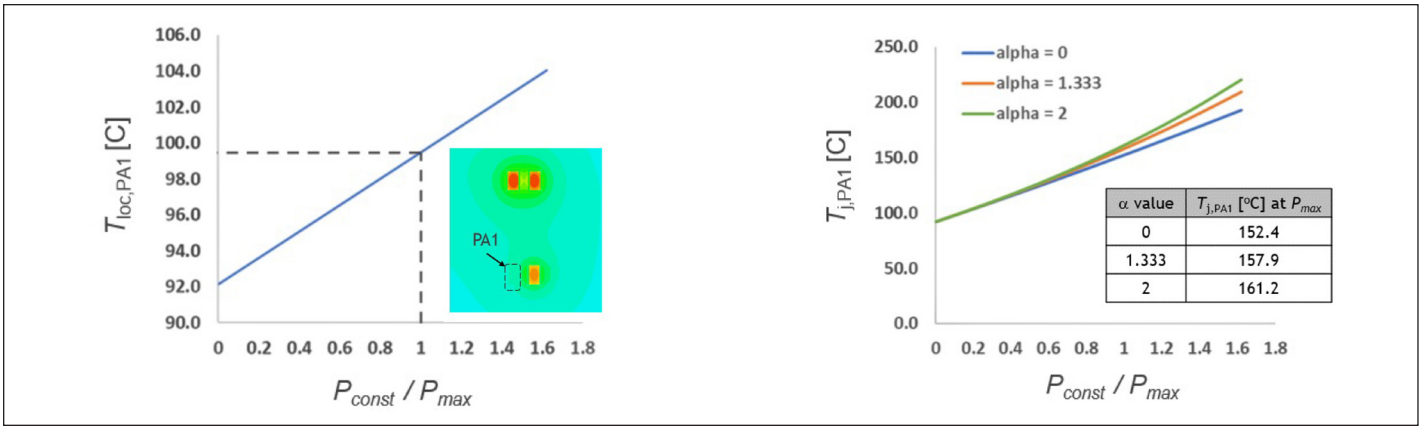


Figure 6: (left) Temperature of silicon local to transistor PA_1 as a function of transistor power P_{const}, with $P_{PA1} = 0$, $P_{PA2} = P_{PA3} = ... = P_{PA8} = P_{const}$. Note temperature contours local to transistor PA_1 shown in the inset image; and (right) Predicted junction temperature for transistor PA_1 as a function of transistor power, as predicted by Eqs. (3) and (4) with various values of α.

ACKNOWLEDGEMENTS

The author would like to acknowledge the excellent collaboration and many useful discussions with Joe Weiner, Yves Baeyens, Pascal Boutet, Pierre Lopez and Shahriar Shahramian.

REFERENCES

[1] Y. Baeyens *et al.*, "A Wideband SiGe BiCMOS Transceiver Chipset for High-performance Microwave Links in the 5.6-43.5 GHz Range," in IEEE Radio Freq. Int. Circ. Symp. (RFIC), 2017.

[2] H. Rucker and B. Heinemann, "SiGe HBT Technology", in *Silicon-Germanium Heterojunction Bipolar Transistors for mm-Wave Systems: Technology, Modeling, and Circuit Applications* (pp. 11-45). N. Rinaldi and M. Schröter, Editors, River Publishers, 2018.

[3] J. C. J. Paasschens *et al.*, "Dependence of thermal resistance on ambient and actual temperature," in *Proc. Bipolar/ BiCMOS Circuits Technol. Meeting, Sep. 12–14, 2004, pp. 108–111*

[4] P. Sun *et al.*, "Flip chip CSP assembly with Cu pillar bump and molded underfill", In *2016 17th International Conference on Electronic Packaging Technology (ICEPT)* (pp. 807-811). IEEE, August 2016.

[5] T. Stander, "A comparison of basic 94 GHz planar transmission line resonators in commercial BiCMOS back-end-of-line processes," in *2014 International Conference on Actual Problems of Electron Devices Engineering (APEDE)*, vol. 1, pp. 185–192, 2014.

[6] https://www.ansys.com/products/electronics/ansys-icepak

Real-Time Prediction of Li-Ion Battery Pack Temperature

Azita Soleymani and William Maltz
Electronic Cooling Solutions, Inc.

The global shift to electric vehicles (EV) is coming and, unless an alternative technology emerges, it will be fueled by high-capacity lithium-ion (li-ion) batteries. Making the hundreds of millions of li-ion batteries the world will eventually need for e-mobility is a massive undertaking full of technical challenges. Concerns about battery pack size, weight, cost and sustainability have to be resolved before there can be a mass rollout of "green" cars. Some of the issues that will be affected by the thermal environment include battery life span and safety. Another benefit, that can result from regulating cell and battery pack temperature within a given range, include an increase in the number of cycles a battery can achieve, making performance more dependable. More importantly, an effective thermal solution reduces the probability of catastrophic battery failure.

Unlike most electronic integrated circuits and microchips in electric vehicles, which operate best at -40˚C to 85˚C or higher, the optimal temperature range for li-ion battery packs is quite narrow and varies depending upon cell supplier, charge and discharge mode and other factors. Both low temperature and high temperature that are outside of this region will lead to degraded performance and irreversible damages, such as lithium plating and thermal runaway.

The thermal requirements of battery packs are specific. Not only the temperatures of the battery cells are important but also the uniformity of the temperature inside the battery cell and within the battery pack are key factors of consideration, in order to deliver a robust and reliable thermal solution. Less temperature

Dr. Azita Soleymani
Dr. Azita Soleymani is a director at Electronic Cooling Solutions Inc. (ECS) and has over 15 years of experience in thermal management. Azita received her PhD in Mechanical engineering at Lappeenranta University of Technology in Finland. She is the co-author to over 30 technical papers. Her expertise includes thermal design of power electronics, consumer electronic products, data center, medical and automotive equipment.

Prior to joining ECS, Dr. Soleymani was thermal-mechanical manager at Byton Inc. where she had the opportunity to develop a thermal solution for Li-ion battery pack in electric cars.

William Maltz
William Maltz is the president and founder of Electronic Cooling Solutions Inc. (ECS) and has over 35 years of experience working on and solving thermal management problems for electronics companies. During his 28 years of consulting, Mr. Maltz has provided thermal management expertise to companies that include: Amazon, AMD, Apple, Boeing, Brocade Communications, any many more.

He has shared technical sessions for Semi-Therm, the Semi-Thermal Thermal Technologies Workshop, ASME InterPACK Conference and the I-Therm Conference. He is also an active member of the Silicon Valley Chapter of the ASME, Semiconductor Thermal Measurement, Modeling, and Management Symposium (Semi-Therm), as well as the program committee for the Semi-Therm Thermal Technologies Workshop.

Mr. Maltz received his Bachelors of Science Degree in Mechanical Engineering from San Jose State University.

uniformity results in the rapid decay of the cycle life of the battery pack. Even worse, a non-uniform temperature distribution may aggravate the unbalanced discharging phenomenon and decrease the available energy for the battery packs.

To evaluate the thermal management system of a li-ion battery pack, the design of experiments (DOE) has to incorporate a range of conditions to ensure that all thermal requirements are met: fast charging, cold start, charging at low temperature, discharging when the charge was low and different drive cycles [1].

Numerical simulation is a powerful tool for evaluating and optimizing a thermal solution at the early stage of design and development [2]. Later, it is used to conduct trouble-shooting. Among the most commonly applied modeling approaches, the electrochemical model provides high accuracy in estimation since it originates from the first principles of underlying electrochemistry. However, accurate estimation is achieved at the cost of high computational power. This makes the method impractical in real-time applications in the battery packs.

In contrast, the equivalent circuit model (ECM) is widely accepted at the application level because of its simplicity and ease in online implementation [3]. ECM utilizes system identification techniques to relate the input and output behaviors of *a battery cell* with circuit elements. All parameters in the ECM are multi-variable functions of State of Charge (SOC), current, temperature, and cycle number. The ECM representation of a battery cell can be used to estimate real-time heat generation and current-voltage (I-V) performance of the battery cell at different operational conditions if the model parameters are well defined [4]. The ECM representation of a battery cell can be integrated within network models of the battery pack to estimate the real-time bulk temperature of cells during different operating scenarios [5]. A network model of the battery pack represents a full battery pack, which includes cells, tabs, electronic connectors, and cooling systems [6]. Such models are typically not sufficiently accurate for thermal analysis and they are primarily used by electrical engineers as part of their electric circuit model.

This article describes a semi-analytical digital twin model of a 90 kW.h li-ion battery pack. The model is used to capture the thermal behavior of the pack in a real-time environment. The paper will demonstrate how the digital twin models of battery packs can be used to perform what-if scenarios, to conduct in-depth root cause analyses, to further optimize the cooling system, to make battery pack life-time predictions and to optimize operating parameters for thermal management. To the knowledge of the authors, this is the first study that utilizes a digital twin model to predict the real time thermal behavior of a full battery pack with high energy capacity of 90 kW.h. The model validation was achieved by comparison of the Digital Twin model results against experimental data over a few dynamic driving profiles.

REAL-TIME HEAT GENERATION RATE

Generation of the digital twin model requires estimation of the real-time heat generation in the battery pack. There are three main sources of heat generation in a *battery pack*, namely ohmic, kinetic and entropic heat. Ohmic heat comprises transport in the wires and connectors, as well as within the battery. Kinetic and entropic heat are due to electrochemical reactions. While kinetic heat is due to reaction at the electrode-electrolyte interface and is therefore always exothermic, entropic heat is due to thermodynamic considerations of the electrochemical reaction and can be exothermic or endothermic.

The heat generation rate in a li-ion battery cell varies as a function the of SOC, temperature and the charge/discharge rate profile. Typically, the heat generated by the li-ion battery cell is estimated from isothermal battery calorimeter testing [7], detailed multi-physics computational fluid dynamics simulations, or ECM approaches. The calorimeter testing is limited to the operational conditions such as SOC, electric current and temperature for which the measurements were carried out. Considering the costs involved and the total number of cases to be measured, calorimeter testing is not feasible for estimating the heat generation rates for a wide range of conditions applicable to the battery packs in EV cars.

The ECM model can meet the real-time implementation requirements; hence it is well suited for Electric Vehicle battery thermal management studies. *Figure 1* illustrates the ECM representation [4] of the lithium-ion batteries used in this study. The two RC networks can be interpreted as a combination of fast and slow time-domain characteristics of the chemical reaction within the battery cell.

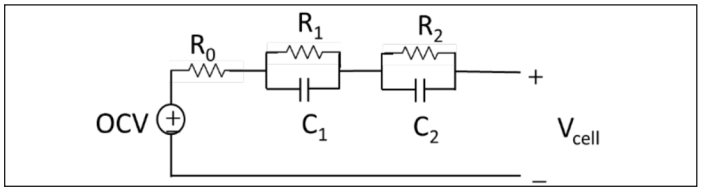


Fig.1 The 2RC model representing the li-ion battery cell performance.

OCV represents the open circuit voltage of the cell. R_0 is the instantaneous response due to the ohmic effect in the battery cell. R_1 and R_2 are the charge transfer resistance and diffusion resistance, respectively.

To obtain the parameters of the 2RC model, Hybrid Pulse Power Characterization (HPPC) experiments were conducted. In order to consider the temperature effect on the cell parameters, HPPC tests were conducted at ten different temperatures (from -20˚C to 60˚C). All parameters were calculated based on these temperatures and at different SOC levels (5% to 100%) and different pulse durations (1 to 30 seconds) for several charging and discharging cycles (c-rate from 0.3 to 6). An algorithm based on the Recursive Least Squares method was developed to calculate the 2RC model parameters from the HPPC test results.

The results of the ECM provide valuable information about cell heat generation rate, terminal voltages, and SOC in real-time, even if the physical sensors embedded inside the battery pack become faulty and or fail for any reason.

To validate the resulted ECM model, a li-ion battery cell was placed in a thermal chamber. The cell was connected to an Arbin battery testing system. This allowed complex real-world EV drive and charge profiles to be precisely replicated and measured. The terminal voltages of the battery cell at different profiles were recorded and the results were compared to the ECM model results at the same operating conditions. Good agreement was observed between the model results and the test data over a wide range of operational conditions. The comparison of the model results against the test data for the US06 drive cycle at 25˚C is depicted in *Fig. 2*. The model predicts the voltage response with an accuracy that is within 25 mV.

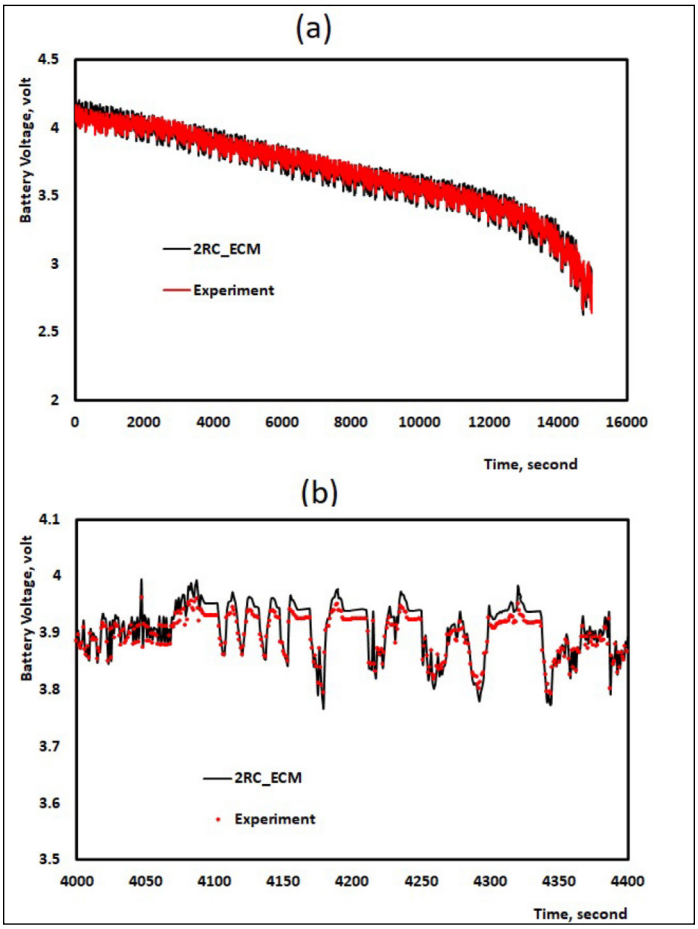


Fig. 2. (a) The variation of the voltage response of a single battery cell initially at 100% SOC to the US06 drive cycle profile. The red and black lines denote the results from test data and the generated 2RC model, respectively. (b) For better visualization, the results are presented in a smaller portion of the US06 drive cycle.

The real time estimation of a single cell heat generation rate at three different temperatures for US06 drive profile is shown in *Fig. 3*. The cell is initially set at 90% SOC and the discharge continues until the SOC reaches 5%. The time required to reach 5% SOC decreases as the temperature decreases. This can be attributed to the fact that the full capacity of a given cell drops with a decrease in temperature. For all three temperatures, an abrupt increase in the heat generation rate toward the end is pronounced. This can be explained by the sudden increase of the internal resistances of the cell at 20% SOCs.

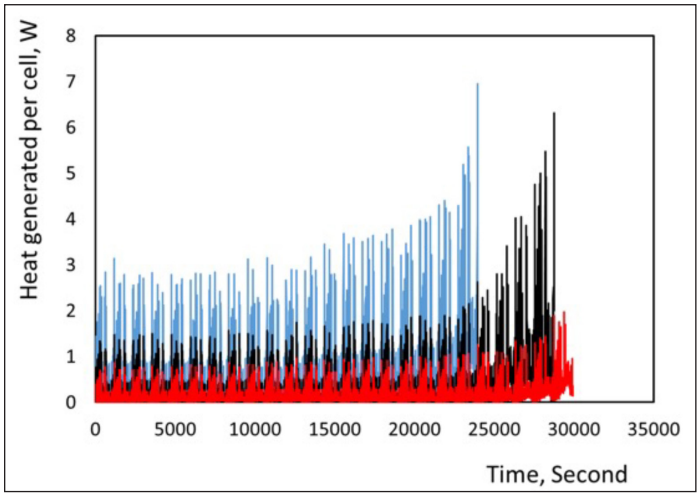


Fig. 3. The estimation of the real-time heat generation rate of a single li-ion battery cell, initially at 100% SOC discharging, according to the US06 drive cycle. Colors are used to indicate the operating temperature at which the cell is kept: red, black and blue denote temperatures of 35, 0 and -10 ˚C, respectively.

DIGITAL TWIN ENABLES REAL-TIME ANALYSES

The methodology used in the present work is shown in *Fig. 4*. A set of transient high-fidelity 3D simulations were performed to generate response curves at the battery pack level. The response curves were then fed into the reduced-order model (ROM) application of commercially available software [8] to create the ROM of the battery pack. Linking the ROM and ECM of the battery cell in a Twin Builder produced a digital twin model of the battery.

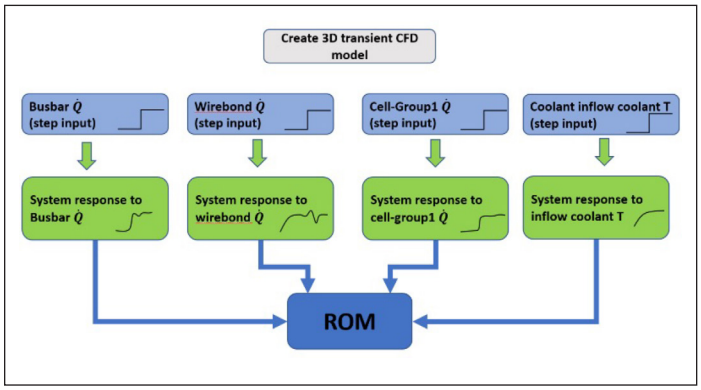


Fig. 4. The workflow used to create the ROMs.

The temperature results from the developed digital twin model of the battery pack were compared to the data obtained from the experiments to validate the digital twin model. *Figure 5(a)* shows the temperature change of the battery pack initially at 90% SOC and 25˚C as the battery pack was discharged at a constant c-rate of 1.5 for 1800 seconds. *Fig. 5(b)* presents the change in the temperature of a 10% SOC battery pack charging for 3000 seconds. As shown in *Fig. 5*, there is excellent agreement between the results obtained from the digital twin model and the experimental results. A maximum difference of 0.7˚C was observed between the digital twin model and the experimental data.

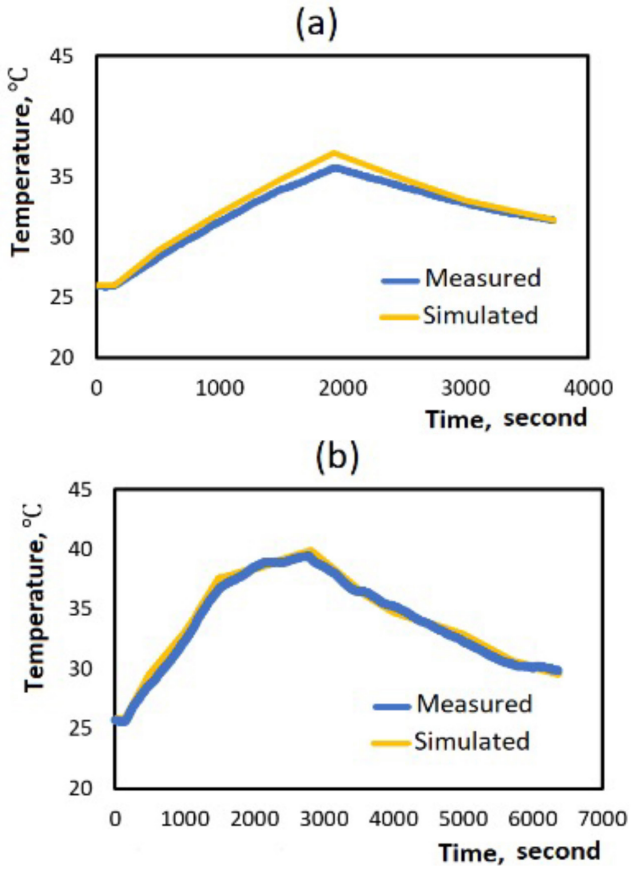


Fig. 5. Temperature versus time at a given location within the battery pack.

The validated digital twin model of the full battery pack was used to evaluate the critical design elements required for an effective thermal monitoring system and significantly reduce the calculation time from weeks to hours, as compared to other approaches. The generated model can be used by non-simulation experts to explore different operating conditions and perform real-time monitoring or predictive maintenance.

APPLICATIONS OF DEVELOPED DIGITAL TWIN

Evaluate the design feasibility of a thermal solution for the battery pack- The generated digital twin model was used to accelerate battery pack design and development by enabling engineers to evaluate design feasibility and to conduct in-depth root cause analyses for various inputs and operating conditions, including initial SOC, temperature, coolant flow rate, different charge and discharge profiles. Every battery pack thermal management design can be evaluated for a wide range of conditions including fast charging, cold start, charging at low temperatures, discharging at different drive cycles. For each scenario, all of the thermal requirements were monitored.

Perform trouble shooting- Live-sensor data was integrated into the digital twin system-level model of the battery pack to create a real-time environment. The generated tool was utilized in the prototype. It was used in validation testing to remotely monitor the real-time temperature of the battery pack and to troubleshoot the test set up. The model acted as a virtual sensor for controllers in which it is hard or impossible to install a sensor.

Position the temperature sensors- The model provided great insight into the temperature profile within the pack at different operating conditions. The results were used to guide the placement of physical monitoring systems.

Optimize the cooling system operating parameters- The generated digital twin model of the battery pack was integrated into a full system level model of the vehicle cooling loops. The resulting model was used to optimize the operating parameters of the cooling loops, as there is a tradeoff between passenger comfort and the battery pack's aging.

Estimate battery pack lifetime- The results of the generated digital model, in conjunction with the empirical models correlating the cell degradation with temperature, were used to estimate the aging of battery packs at different ranges of long-term operating conditions.

The semi-analytical digital twin model operating in real-time was used to perform what-if scenarios, to conduct in-depth root cause analyses and to estimate the lifetime of the battery pack. Further, the model was used to develop and optimize the operating setup of the vehicle cooling loops for user comfort and safety. The reliability and the low computational cost of the developed model significantly reduced the time required for optimizing and troubleshooting the battery pack thermal system. This also resulted in a significant reduction in the time-to-market.

REFERENCES

[1] Yang X-G., Zhang G., Ge S., Wang C-Y., Fast charging of lithium-ion batteries at all temperatures. =Proceedings of the National Academy of Sciences. 115(2018) 7266-7271.
[2] D. Ghosh, Maguire, and D. X. Zhu, Design and CFD Simulation of a Battery Module for a Hybrid Electric Vehicle Battery Pack, SAE paper 2009-01-1386.
[3] Hu, X., Lin, S., Stanton, S., and Lian, W., A State Space Thermal Model for HEV/EV Battery Modeling, SAE Technical Paper 2011-01-1364.
[4] Rahmoun, Ahmad & Biechl, Helmuth, Modelling of Li-ion batteries using equivalent circuit diagrams. Przeglad Elektrotechniczny. 88(2012) 152-156.
[5] Yen, C., Han, T., Kaushik, S., and Khalighi, B., Application of CAEBAT System Approach for a Liquid-Cooled Automotive Battery Pack, SAE Technical Paper 2016, 01-1205
[6] L. Gao, S. Liu, and R. A. Dougal, Dynamic Lithium-Ion Battery Model for System simulation, IEEE Trans. Comp. Package. Technology, vol. 25, No 3 (2002) 495-505.
[7] Pesaran, A. Battery Thermal Management in EVs and HEVs: Issues and Solutions. Battery Man. 43(2001).
[8] Ansys DesignXplorer's 3D ROM builder, www.ansys.com

Statistics Corner: Regression Analysis

Ross Wilcoxon
Associate Technical Editor

Throughout their careers, engineers and scientists are all likely to encounter and utilize the results of regression analysis, which is "a set of processes for estimating the relationships between a dependent variable and one or more independent variables" [1]. In other words, regression analysis uses a set of data to estimate a relationship between the independent 'predictor(s)' and a 'response' or 'output' parameter. In its simplest form, a response, y, may be linearly related to a single predictor, x, in a relationship of y = mx + b. Regression analysis provides a method for estimating values of the constants m (the slope) and b (the intercept).

Regression analysis can be accomplished with different approaches that could include, at least theoretically, a piece of wood, drywall screws, rubber bands and a welding rod[1], as shown in *Figure 1*. In this regression analysis, screws were put into x-y locations of a graph drawn on the wood and rubber bands between the welding rod and the screws hold the welding rod in an equilibrium position that allow the slope and the intercept to be determined.

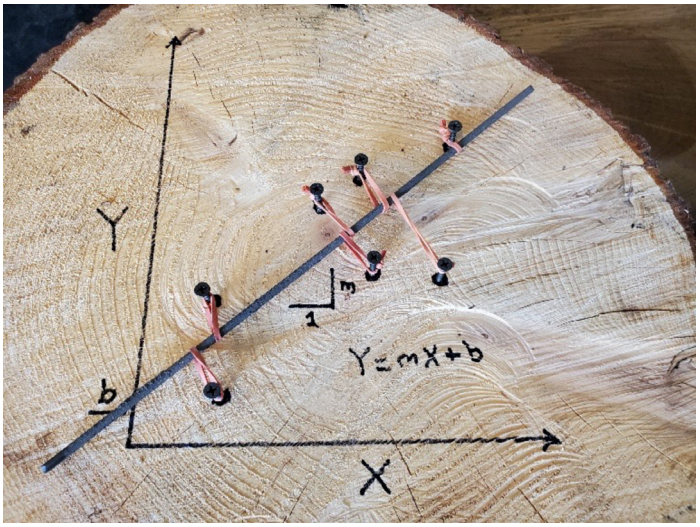


Figure 1. Regression analysis done the hard way

A slightly easier and certainly more accurate approach for conducting a regression analysis is the use of Least Squares. In this approach, rather than the location of the welding rod that leads to a balance in the forces generated by the rubber bands in *Figure 1*, the 'welding rod' corresponds to the straight line that produces the smallest value of E, where E is the sum of squares of the distance in the y-direction between the line and each data point. The equations for calculating the coefficients for a least-squares estimate for linear regression with a single predictor, i.e., y = mx + b, are shown in *Equations {1}* and *{2}* [2]:

$$m = \frac{S_{xy}}{S_{xx}} = \frac{\sum(x_i-\bar{x})(y_i-\bar{y})}{\sum(x_i-\bar{x})^2} \quad \{1\}$$

$$b = \bar{y} - m\bar{x} \quad \{2\}$$

where x_i and y_i are the x-y values for the ith data point and $\bar{x}$ and $\bar{y}$ are the mean values of the x and y data respectively. The coefficient of determination, R^2, is another important parameter in regression analysis. This term describes how well the regression analysis describes the data: an R^2 of 1 indicates a perfect fit while a value of 0 indicates that the regression analysis does not predict the response from the input data. R^2 is calculated using *Equation {3}*:

$$R^2 = \frac{S_{yy}-SSE}{S_{yy}} = \frac{\sum(y_i-\bar{y})^2-\sum(y_i-b-mx_i)^2}{\sum(y_i-\bar{y})^2} \quad \{3\}$$

where SSE is known as the sum of squares error.

Equations {1-3} are implemented in any software that does regression analysis. For example, several methods can be used in Microsoft Excel to determine regression coefficients. Methods that this author has used are summarized in *Figure 2*. *Figure 3* shows an example of an Excel regression analysis, using Option 1 as described in *Figure 2*, for the x-y values that were used in the demonstration illustrated in *Figure 1*.

[1] In other words, random stuff that I had laying around my house on a weekend.

For one independent variable:

Option 1.
Create an x-y chart of the data being analyzed, right click on the data the chart, select "Add Trendline…", check boxes for "Display Equation on Chart" and "Display R-squared on chart"

Option 2.
Enter the functions "=slope(y-values, x-values)", "=intercept(y-values, x-values)", and/or "=rsq(y-values, x-values)", where 'x-values' and 'y-values' are cells that contain the x and y values of the data set being analyzed.

For one or more independent variables (multiple x's):

Option 3.
Highlight a suitable range of cells, type in the function "=linest(y-values, x-values, true, true)", and instead of hitting 'Enter' hit Control-Shift-Enter, because this is an array formula. Relevant statistics are generated in the array (the correct size of the array depends on how many sets of x-values are selected) (note, the configuration of the output parameters does not correspond with the input configuration, so it is recommended that before using this function for the first time, they generate a dummy set of data with known coefficients so that they can know exactly where the important output values are in the generated array).

Option 4.
Add the Data Analysis Add-in, go to the 'Data' tab, select 'Data Analysis' to open a pick list of data analysis tools, select 'Regression' and define inputs in the dialogue box that is displayed.

Option 5:
Guess coefficients for each independent variable and put them into a range of cells. Calculate the value of y using these coefficients for each set of x-values and sum the error for each data point, i.e., the square of the difference between measured y and calculated y. Then use the Excel Solver Add-in to minimize that sum by varying coefficients. Depending on how good the initial guessed coefficient values are and the nature of the modeled regression curve, this approach may converge to the correct values or may spiral off to 'infinity and beyond'.

Figure 2. Methods for Regression Analysis in Excel:

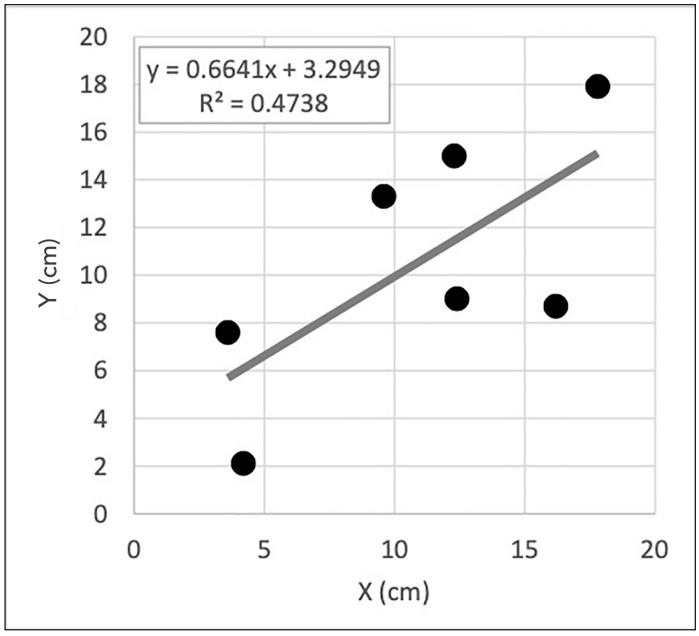


Figure 3. Excel-based regression analysis for same data as Figure 1

A previous column in this series described how probability distribution concepts could be used to a confidence interval for a limited set of data. When measurements are used to determine an average value, we can determine what range of values the actual average of the falls within a range to a given confidence level [3]. The confidence interval depends on the variance of the measurements (standard deviation) and the number of measurements made. The t-distribution was used in the calculation of the range.

In the same manner that we estimate a mean value within a confidence interval, confidence intervals also apply to the coefficients (slope and intercept) determined through regression analysis. These intervals are determined with *Equations {4}* and *{5}* [2]:

Confidence band on the slope: $m \pm t_{\alpha/2} \frac{S}{\sqrt{S_{xx}}}$ {4}

Confidence band on the intercept: $b \pm t_{\alpha/2} \frac{S\sqrt{\sum x^2}}{\sqrt{nS_{xx}}}$ {5}

Where $t_{a/2}$ is the t-distribution corresponding to the confidence level and degrees of freedom, n is the number of data points, Σx^2 is the sum of all x values, $S_{xx} = \sum(x_i - \bar{x})^2$, and S = SSE/(n-2) = $\frac{\sum(y_i - b - mx_i)^2}{n-2}$.

Another confidence interval of interest is the value of y that is predicted by the regression analysis for any x-value. This confidence interval accounts for the combined effects of the confidence bands associated with the slope and intercept and is shown in *Equation {6}*.

Confidence band on y-value: $y = mx + b \pm t_{\alpha/2} S \sqrt{A + \frac{1}{n} + \frac{(x-\bar{x})^2}{S_{xx}}}$ {6}

Where A = 0 if we are estimating the confidence band on the average y value for the population tested and A = 1 for an individual item.

Data from the heat sink assessment discussed in [4] will illustrate how these equations are used to determine confidence intervals of regression coefficients. A flat plate heat sink was tested in still air under a range of orientations relative to gravity. Results for ~20W dissipation values for a range of angles are shown in *Figure 4*, which includes regression analysis results with R^2 of ~86%. While this R^2 value is reasonable, the suitability of the fit is probably somewhat questionable: the values at the low and high range of measurements are above the fit while those in the middle are below. This is often an indication that the regression analysis may not be capturing the fundamental physics that influence the results.

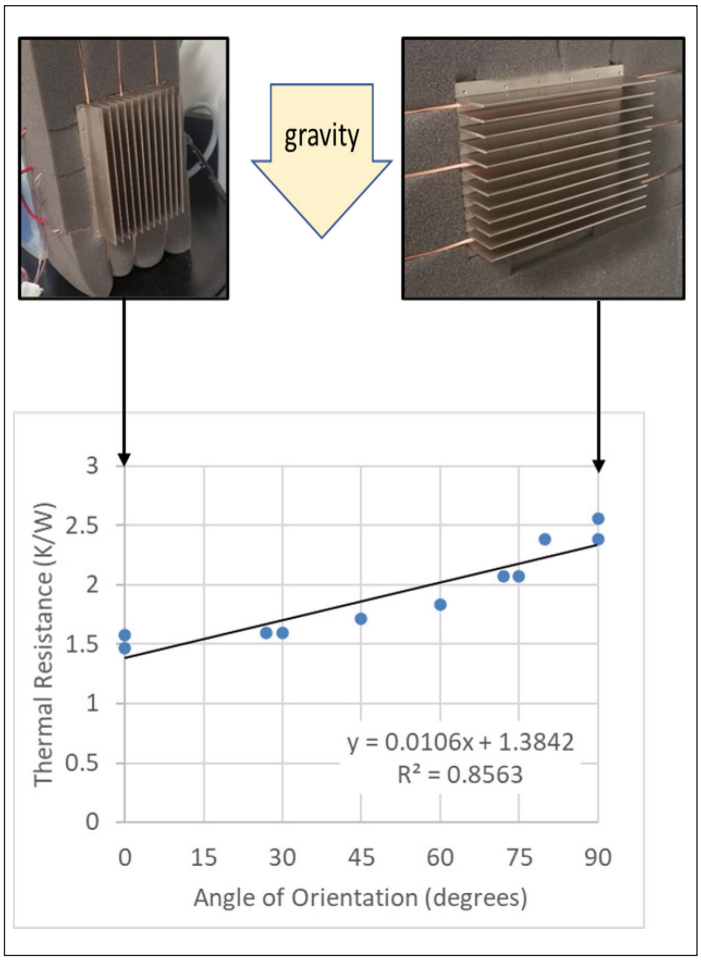


Figure 4. Test data for natural convection heat sink at different orientations

When assessing the results in terms of the physics that cause the heat sink thermal resistance to change with its orientation relative to gravity, it seems reasonable that the buoyant flow that drives natural convection will depend on the cosine of the orientation angle, rather than the angle itself. *Figure 5* shows the resulting correlation between the thermal resistance as a function of the cosine of its angle relative to gravity. This appears to improve the fit substantially; the R^2 increases from 86% to 95%. Given this improvement in the fit, the subsequent analysis assumes that the cosine of the angle, rather than the angle itself, is the correct independent variable for regression analysis.

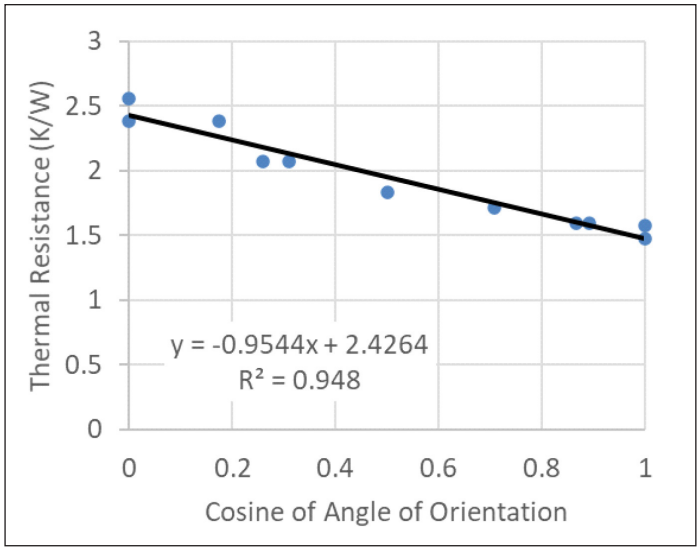


Figure 5. Natural convection heat sink resistance vs. cosine of orientation

Table 1 shows the eleven data points used to generate the previous plots while the values of the parameters used in, or resulting from, the regression analysis are shown in *Table 2* along with brief descriptions of how they are calculated.

Θ (deg)	cos(Θ)	R_{th} (K/W)
0	1.000	1.575
45	0.707	1.711
60	0.500	1.835
30	0.866	1.591
27	0.891	1.594
75	0.259	2.069
90	0.000	2.380
0	1.000	1.472
72	0.309	2.074
80	0.174	2.383
90	0.000	2.561

Table 1. Measured data

Parameter	Value	Equation
n	11	number of data points
μ_x	0.519	average of all x values
μ_y	1.931	average of all y values
S_{xx}	1.527	sum of each value of $(x-\mu_x)^2$
S_{yy}	1.467	sum of each value of $(y-\mu_y)^2$
S_{xy}	-1.457	sum of each value of $(x-\mu_x)^*(y-\mu_y)$
Σx^2	4.487	sum of each value of x^2
m	-0.954	$= S_{xy} / S_{xx}$
b	2.426	$= \mu_y - m^*\mu_x$
SSE	0.0764	sum of each value of $(y - b - mx)^2$
R^2	94.8%	$= (S_{yy} - SSE)/ S_{yy}$
S	0.0921	= SSE/(n-2)

Table 2. Calculated parameters for the regression analysis confidence interval

The confidence intervals for the regression coefficients depend on what confidence level is defined. For example, for a 95% confidence level, the t-statistic would be calculated for a probability of 0.975 (1-(1-0.95)/2) and 9 degrees of freedom (sample size of 11 minus 2) as 2.262. The confidence bands for the coefficients are then:

Slope confidence band: $\pm t_{\alpha/2}\frac{S}{\sqrt{S_{xx}}} = 2.262 * \frac{0.0921}{sqrt(1.527)} = 0.169$

Intercept confidence band: $\pm t_{\alpha/2}\frac{S\sqrt{\sum x^2}}{\sqrt{nS_{xx}}} = 2.262 * \frac{0.0921*sqrt(4.487)}{sqrt(11*1.527)} = 0.110$

Since the nominal slope and intercept are -0.954 and 2.426, respectively, we can be 95% confident that the slope is between -1.123 and -0.786 (i.e., -0.954±0.169) and the intercept is between 2.317 and 2.536. Using *Equation {6}*, we can determine the confidence bands for the population and individual measurements, which are plotted in *Figure 6*.

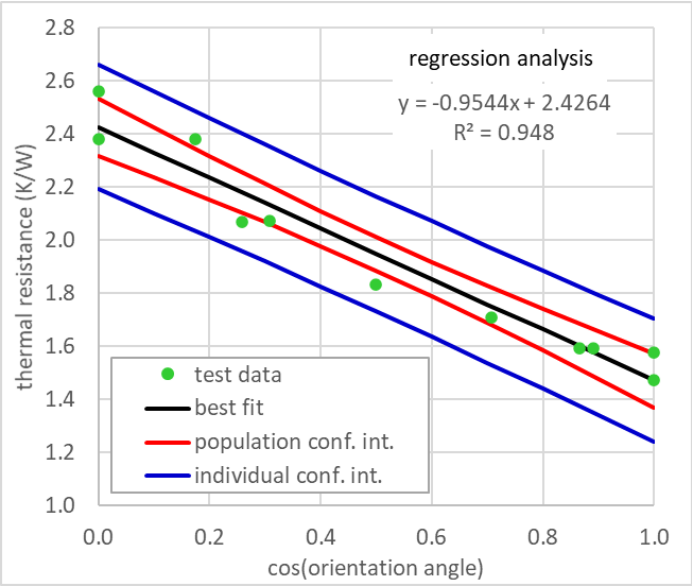


Figure 6. Confidence bands for regression analysis of heat sink

In summary, conducting a regression analysis can be a relatively straightforward process. Tools are widely available, or the basic equations can easily be implemented into a spreadsheet, to determine a curve fit between independent and dependent variables. One needs to keep in mind, however, that these tools will provide a curve fit, regardless of whether the correct variables have been input to them. As in this case, recognizing the physics of the situation led to a change in the independent variable so that a better fit was obtained. Also, this article described how to calculate confidence bands for the coefficients resulting from a regression analysis, since one must recognize that those values are merely estimates.

REFERENCES

- https://en.wikipedia.org/wiki/Regression_analysis (accessed 8/7/21)
- J. S. Milton and Jesse Arnold, *Introduction to Probability and Statistics: Principles and Applications for Engineering and the Computing Sciences*, McGraw-Hill, 1986
- Ross Wilcoxon, "Statistics Corner – Confidence Intervals", *Electronics Cooling Magazine*, Spring 2021
- Ross Wilcoxon, "Statistics Corner – Comparing Populations", *Electronics Cooling Magazine*, Summer 2021

Summary of the IEEE ITherm 2021 Conference

John F. Maddox
University of Kentucky, Paducah

The IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm) was held virtually June 1-4, 2021. This was the 20th ITherm, which was first held in 1988. The conference was historically held every other year until 2016 when it switched to an annual schedule. ITherm 2021 was sponsored by the IEEE Electronics Packaging Society (EPS). ITherm has partnered with IEEE EPS peer conferences, including the International Workshop on Thermal Investigations of ICs and Systems (THERMINIC) in Europe, and the Electronics Packaging Technology Conference (EPTC 2021) in Asia.

The ITherm 2021 program consisted of 14 professional development workshops and three full days of technical presentations in four tracks with 41 sessions in which 159 papers were presented. Additional technical events included three keynote addresses, five panels, five technology talks, a student poster competition, a student heat sink design competition, and a student overclocking competition. There was also a panel held jointly with ECTC–ECTC/ITherm Diversity Panel, "Diversity Does Matter and Can Drive Enhanced Business Performance."

KEYNOTES

On the first day of the conference, Dr. Jonathan Koomey, founder of Koomey Analytics, gave a keynote address entitled "That Does Not Compute: Facts and Fiction About Computing and the Environment" discussing the challenges in obtaining accurate and up-to-date information on the electricity use and environment impact of information technology (IT).

On the second day of the conference, Dr. Theodore Sizer, Executive Vice President of Smart Optical Fabric and Device Research in Nokia Bell Labs, gave a keynote address entitled "The Lasting Impact and New Challenges for our Communication Network" describing the challenges and opportunities posed by the coming 5G Industrial Revolution.

On the final day of the conference, Dr. Jayathi Murthy, Ronald and Valerie Sugar Dean at the UCLA Henry Samuel School of Engineering and Applied Science, gave a keynote address entitled "Engineering the Time of Corona: Some Lessons for the Future" discussing the impacts of the pandemic on engineering education and research.

BEST AND OUTSTANDING PAPERS

Awards given for the best and outstanding papers in each track, based on judging from reviews and inputs from session and track chairs, were unveiled to the attendees.

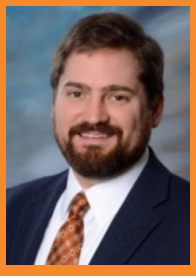
BEST PAPERS

Component Level Thermal Management

- Karthekeyan Sridhara, Vinod Narayanan, and Sushil Bhavnani, "Development of Microgravity Boiling Experiments aboard the International Space Station from Terrestrial Adverse Gravity Outcomes for a Ratcheted Microstructure with Engineered Nucleation Sites," Auburn University and University of California – Davis, p317.

System Level Thermal Management

- Prabhakar Subrahmanyam, Pooya Tadayon, Ying-Feng Pang, Arun Krishnamoorthy, and Amy Xia, "On the Thermal Effi-



Dr. John F. Maddox
Dr. John F. Maddox is an Associate Professor of Mechanical Engineering at the University of Kentucky, Paducah Campus. He received his Ph.D. in mechanical engineering from Auburn University in 2015. His primary research areas are thermal management of high-power electronics through jet impingement and thermal characterization of advanced materials used in aerospace and electronics cooling applications. He may be contacted at john.maddox@uky.edu

ciencies of Cascading Heat Exchangers: An Experimental Approach – I," Intel Corporation, p382.

Mechanics and Reliability
- Pradeep Lall, Tony Thomas, and Ken Blecker, "Prognostic and RUL Estimations of SAC105, SAC305, and SnPb Solders under Different Drop and Shock Loads using Long Short-Term Memory (LSTM) Deep Learning Technique," Auburn University and US Army CDDC-AC, p255.

Emerging Technologies & Fundamentals
- Pradeep Lall, Jinesh Narangaparambila, Kyle Schulze, and Curtis Hill, "Process Recipes for Additively Printed Copper-Ink Flexible Circuits using Direct Write Methods," Auburn University and NASA Marshall Space Flight Center, p231.

BEST PAPER – RUNNER UP

Component Level Thermal Management
- Palash V Acharya, Manojkumar Lokanathan, Abdelhamid Ouroua, Robert Hebner, Shannon Strank, and Vaibhav Bahadur, "Assess the Impact of Novel Polymers and Thermal Management in a Power Electronics Module Using Machine Learning Approaches," University of Texas at Austin and Army Research Lab South, p114.

System Level Thermal Management
- Raffaele L. Amalfa, Francois P. Faraldo, Todd Salmon, Ryan Enright, Filippo Cataldo, Jackson B. Marcinichen, and John R. Thome, "Hybrid Two-Phase Cooling Technology for Next-Generation Servers: Thermal Performance Analysis," Nokia Bell Labs, Provides Metalmeccanica S.r.l, and JJ Cooling Innovation, p285.

Mechanics and Reliability
- Venkatesh Avula, Vanessa Smet, Yogendra Joshi, and Madhavan Swaminathan, "Augmented Finite Element Method (AFEM) for the Steady-State Thermal and Thermomechanical Analysis of Heterogeneous Integration Architectures," Georgia Institute of Technology, p232.

Emerging Technologies & Fundamentals
- Adam A Wilson, Darin Sharar, Jay R. Maddux, Michael Fish, and Ian Kierzewski, "Toward High-Throughput Thermal Characterization of Combinatorial Thin-Film Solid State Phase Change Materials," US Army Research Laboratory and General Technical Services, p373.

STUDENT POSTER AND NETWORKING SESSION

The student poster and networking session provided an opportunity for students to interact with industry and academic leaders in their fields. This venue enabled students to connect with possible future employers and to receive feedback on their work. The student posters were subjected to two rounds of judging based on technical merit, clarity, self-sufficiency of the content, originality of the work, visual presentation, and oral presentation with best and outstanding posters selected for each technical track and one poster was selected as the best overall.

Best Overall Poster
- Venkatesh Avula, Georgia Institute of Technology "Augmented Finite Element Method (AFEM) for Steady-state Thermal and Thermomechanical Modeling Integration Architectures"

BEST POSTERS

Component Level Thermal Management
- Meghavin Bhatasana, Purdue University "Optimization of an Embedded Phase Change Material Cooling Strategy Using Machine Learning"

System Level Thermal Management
- Achutha Tamraparni, Texas A&M University "Experimental Validation of Composite Phase Change Material Optimized for Thermal Energy Storage"

Mechanics and Reliability
- Venkatesh Avula, Georgia Institute of Technology "Augmented Finite Element Method (AFEM) for Steady-state Thermal and Thermomechanical Modeling Integration Architectures"

Emerging Technologies & Fundamentals
- Pranay Nagrani, Purdue University "Two-Fluid Modeling of Dense Particulate Suspensions for Electronics Cooling"

OUTSTANDING POSTERS

Component Level Thermal Management
- Soumya Bandyopadhyay, Purdue University "Experimental Characterization of Cascaded Vapor Chambers for Spreading of Non-Uniform Heat Loads"

System Level Thermal Management
- Ujash Shah, UCLA "Segmented Thermal Management with Flash Cooling for Heterogeneous Wafer-Scale Systems"

Mechanics and Reliability
- Padmanava, Auburn University "Effect of Surface Preparation and Cure-Parameters on the Interface Properties of Flexible Encapsulation in FHE Applications"

Emerging Technologies & Fundamentals
- Saeel Shrivallabh Pai, Purdue University "A Machine-Learning-Based Surrogate Model for Internal Flow Nusselt Number and Friction Factor in Various Channel Cross Sections"

STUDENT HEAT SINK DESIGN CHALLENGE

The ASME K-16/IEEE EPS Student Design Challenge is a team competition in which students design, analyze, and optimize an additively manufactured, aluminum heat sink to cool a constant heat flux power electronics module subject to natural convection. Designs were submitted by teams from around the world and evaluated by a team of experts based on a series of design and manufacturing criteria. For the 2021 competition, the top 8 most effective and creative designs were printed using additive manufacturing facilities at GE and tested using state-of-the-art test equipment at Oregon State University. The 8 finalist heat sinks are shown in *Figure 1*.

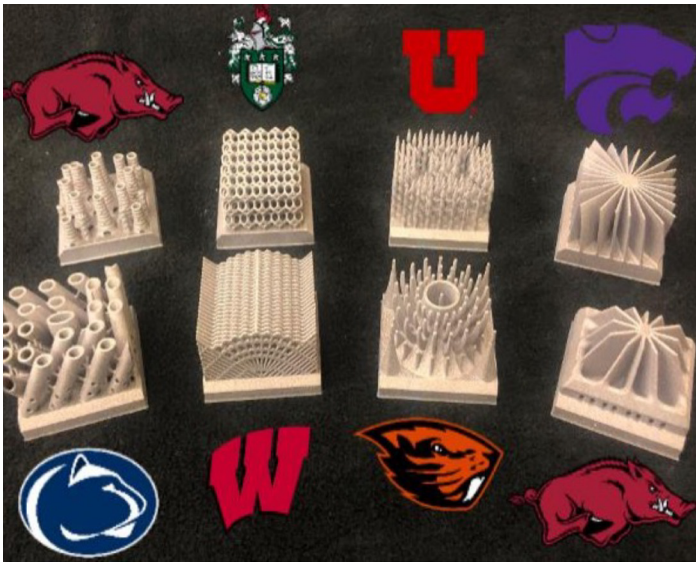


Figure 1: Heat sink design challenge finalists. [Top row left to right: University of Arkansas, University of Leeds (UK), University of Utah, Kansas State University; Bottom row left to right: Pennsylvania State University, University of Wisconsin, Oregon State University, University of Arkansas]

WINNER

- Toposink, University of Utah: Carter Cocke, Bence Csontos, Travis Allen, Eric Steenburgh, Michael Alverson, and Hunter Scott (*Figure 2*)

RUNNER-UP

- Hot Hogs, University of Arkansas: Hayden Carlton, Reece Whitt, Whit Vinson, Brooks Barlow, Sergio Romero Melgar (*Figure 3*)

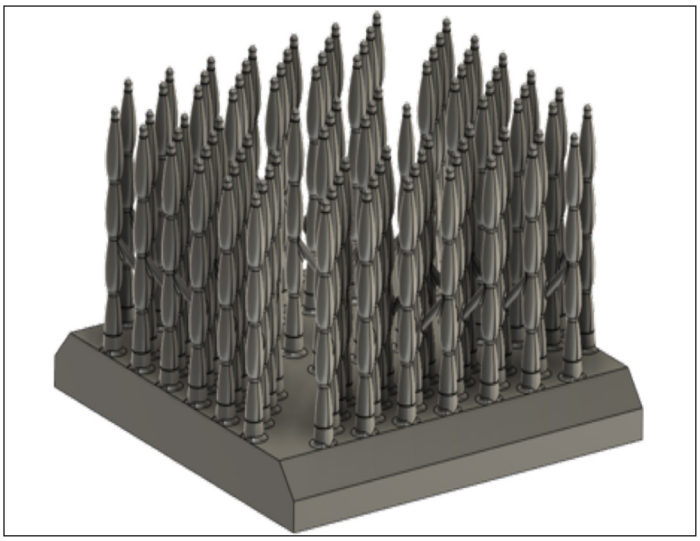


Figure 2: Winning Design - University of Utah

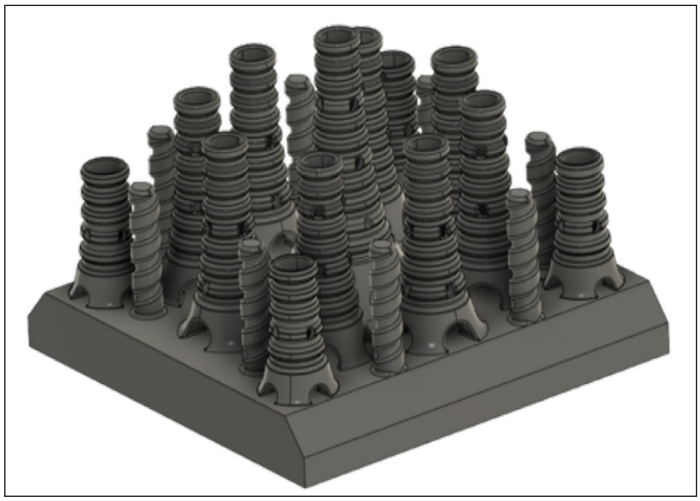


Figure 3: Runner-up - University of Arkansas

STUDENT OVERCLOCKING COMPETITION

In the IEEE EPS Student Overclocking Competition, which was a new event for ITherm 2021, student teams designed, built, and tested a thermal management solution to enable the overclocking of a processor. The student teams were given the opportunity to describe their designs and report the overclocking performance using competition-standard benchmarks. Teams described the engineering aspects necessary to perform the overclocking through short presentations. *Figure 4* shows a liquid nitrogen cooled overclocking system developed by students at Purdue University who were declared the winners of the 2021 competition. The long-term goal is to grow the competition into an Intercollegiate Overclocking (IOC) League with qualifying rounds leading to live in-person competitions. If you are interested in starting an overclocking team at your university, please submit an interest form here[1].

Figure 4: Purdue overclocking system (Photo courtesy of Jared Pike, Communication Specialist, School of Mechanical Engineering, Purdue University)

[1] For those readers seeing this in the print version, the hyperlink is: https://docs.google.com/forms/d/e/1FAIpQLSdYFkW9RmU2iJ98cVNWxhtZMhDK1ZKjUdbaie02qoB_a6yY5Q/viewform

RICHARD CHU ITHERM AWARD FOR EXCELLENCE

Prof. Cristina Amon was awarded the Richard Chu ITherm Award for Excellence. Prof. Amon is Alumni Distinguished Professor and Dean Emerita of the Faculty of Applied Science and Engineering at the University of Toronto. She has pioneered developments in computational fluids dynamics, multidisciplinary multiscale hierarchical modelling, concurrent design, and optimization methodologies for thermo-fluid transport phenomena, with applications to thermal management of electronics and electric vehicles, renewable energy, and biomedical devices.

PROCEEDINGS

We are also pleased to announce that the ITherm 2021 Proceedings are available through IEEE Xplore Digital Library at https://ieeexplore.ieee.org/xpl/conhome/9502930/proceeding. Papers appearing in the Table of Contents are available for access and download, along with listings of our Keynote Speakers, Tech Talks, Panels, Sponsors, and Exhibitors.

ITHERM 2022

We hope you will join us at the Sheraton Hotel and Marina in San Diego, CA May 31st-June 3rd, 2022, for ITherm 2022. Abstracts for the ITherm 2022 conference will be due on Sept 20th, 2021.

ITherm SAN DIEGO, CA 2022

SPONSORS AND EXHIBITORS

ITherm 2021 was made possible by those of you who attended and by the generous support of our sponsors and exhibitors.

ITHERM 2021 ORGANIZATION COMMITTEE

Justin Weibel, Ph.D.
Purdue University
General Chair

Dustin Demetriou, Ph.D.
IBM
Program Chair

Satish Kumar, Ph.D.
Georgia Tech
Vice Program Chair

Ashish Gupta, Ph.D.
Intel Corporation
Communications Chair

TECHNICAL EDITORS SPOTLIGHT

Meet the 2021 *Electronics Cooling*® Editorial Board

VICTOR CHIRIAC, PhD | GLOBAL COOLING TECHNOLOGY GROUP

Associate Technical Editor

A fellow of the American Society of Mechanical Engineers (ASME) since 2014, Dr. Victor Adrian Chiriac is a co-founder and a managing partner with the Global Cooling Technology Group since 2019. He previously held technology/engineering leadership roles with Motorola (1999-2010), Qualcomm (2010 - 2018) and Huawei R&D USA (2018 - 2019). Dr. Chiriac was elected Chair of the ASME K-16 Electronics Cooling Committee and was elected the Arizona and New Mexico IMAPS Chapter President. He is a leading member of the organizing committees of ASME/InterPack, ASME/ IMECE and IEEE/CPMT ITherm Conferences. He holds 19 U.S. issued patents, 2 US Trade Secrets and 1 Defensive Publication (with Motorola), and has published over 107 papers in scientific journals and at conferences.

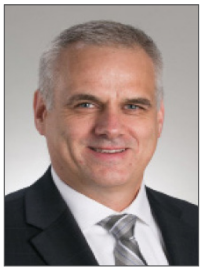
► vchiriac@gctg-llc.com

GENEVIEVE MARTIN | SIGNIFY

Associate Technical Editor

Genevieve Martin (F) is R&D manager for thermal & mechanics competence at Signify (former Philips Lighting), The Netherlands. She is working in the field of cooling of electronics and thermal management for over twenty years in different application fields. From 2016 to 2019, she coordinates the European project Delphi4LED (3 years project) dealing with multi-domain compact model of LEDs. She served as General chair of Semitherm conference and is an active reviewer and technical committee in key conferences Semi-Therm®, Therminic, Eurosime.

► genevieve.martin@signify.com



ROSS WILCOXON | COLLINS AEROSPACE ADVANCED TECHNOLOGY

Associate Technical Editor

Dr. Ross Wilcoxon is a Technical Fellow in the Collins Aerospace Advanced Technology group. He conducts research and supports product development related to component reliability, electronics packaging and thermal management for communication, processing, displays and radars. He has more than 40 journal and conference publications and is an inventor on 30 US Patents. Prior to joining Rockwell Collins (Now Collins Aerospace) in 1998, he was an assistant professor at South Dakota State University.

► ross.wilcoxon@collins.com

Index of ADVERTISERS

Alpha Novatech, Inc.
473 Sapena Ct. #12,
Santa Clara, CA 95054

t: +1 (408) 567-8082
e: sales@alphanovatech.com
w: www.alphanovatech.com
page: 2

Electronics Cooling
1000 Germantown Pike,
Plymouth Meeting, PA 19462

t: (484) 688-0300
e: info@electronics-cooling.com
w: www.electronics-cooling.com
page: 21

Malico Inc.
No. 5 , Ming Lung Road
Yang Mei
Tao Yuan 32663

t: (886) 3-4728155
e: inquiry@malico.com
w: www.malico.com
page: 5

Schlegel EMI
1600 Lexington Ave
Suite 236A
Rochester, NY 14606

t: 585-643-2000
e: schlegelemi.na@schlegelemi.com
w: www.schlegelemi.com
page: 20

SIEMENS Digital Industries Software
8005 SW Boeckman Road
Wilsonville, OR 97070

t: (800) 592-2210
e: www.plm.automation.siemens.com/global/en/contact-us.html
w: www.plm.automation.siemens.com/global/en/
page: 11

THERMAL LIVE
Online Event
October 19-20, 2021

t: (484) 688-0300
e: info@electronics-cooling.com
w: www.thermal.live
page: 36

thermalLIVE™

THE EXPERIENCE

ThermalLIVE is a free, 3-day online event for electronics and mechanical engineers in the thermal management space to learn about the latest innovations, trends, and challenges directly from industry thought leaders.

Past topics have included advanced thermal techniques in power electronics, design and manufacturing of blind mate couplings, selecting TIMs for different applications, calculations and design elements for liquid cooling, and more.

JOIN US FOR OUR 7TH YEAR!
REGISTRATION IS OPEN NOW!

thermal.live
https://thermal.live/