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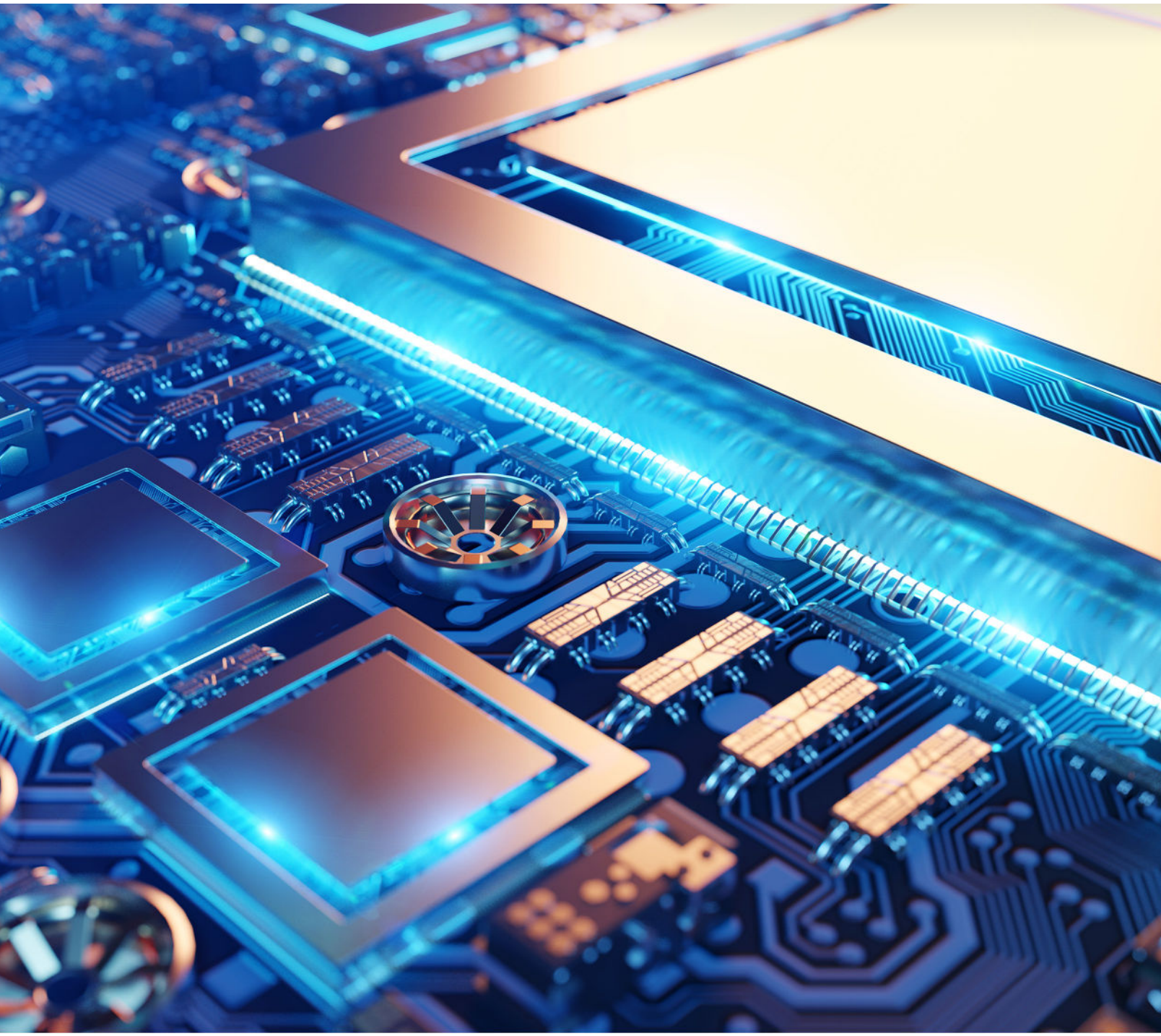
2022 SIGNAL & POWER INTEGRITY GUIDE



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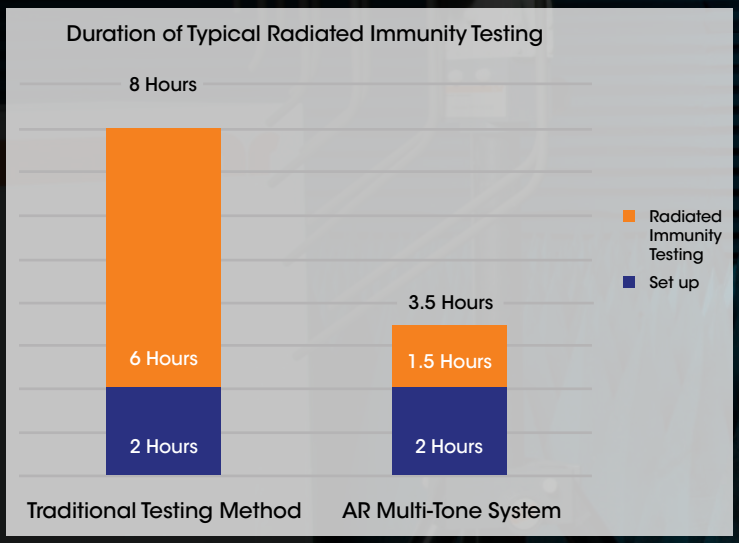

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FIVE TECHNIQUES FOR FAST, ACCURATE POWER INTEGRITY MEASUREMENTS

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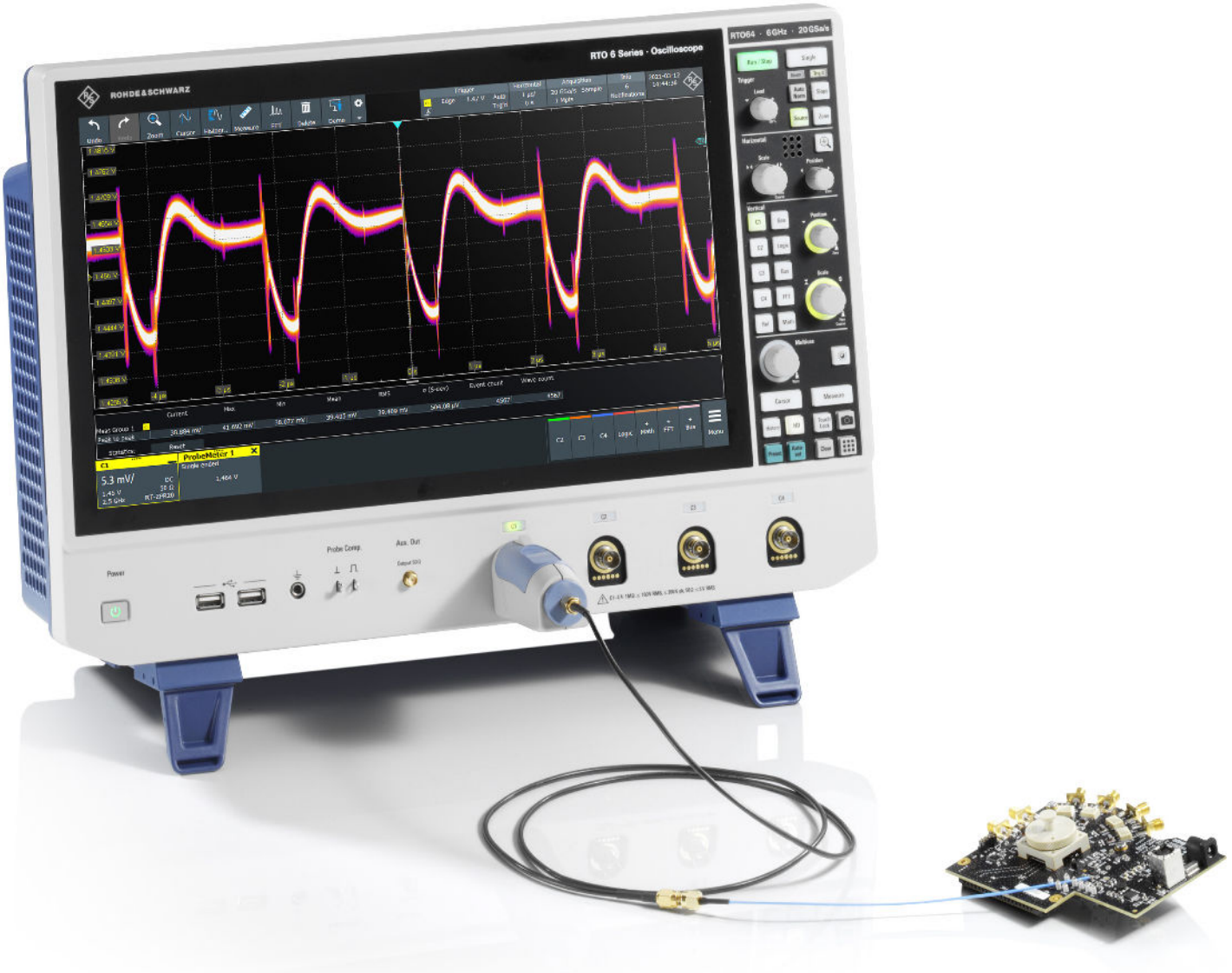
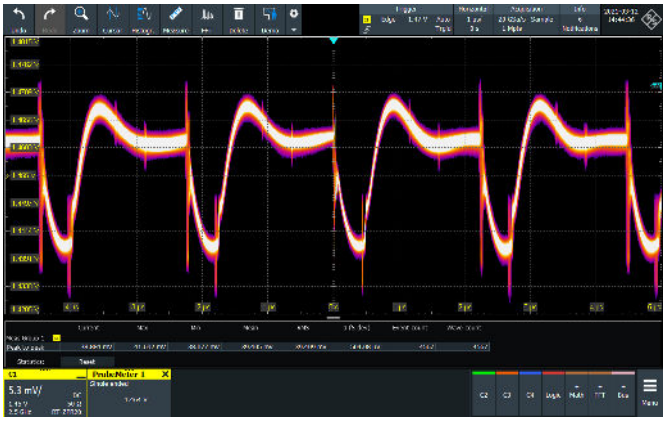


Rail voltages are getting smaller, and tolerances are decreasing. As a result, making accurate power rail measurements has become much more difficult. In the past, any oscilloscope was able to measure ripple on historical 5 V rails with 10% tolerance, since the 500 mV requirement was well above the noise level of the oscilloscope.

Industry dynamics are driving both a decrease in rail voltage values as well as tighter tolerances across a wide range of rails. Making an accurate ripple measurement on a 1 V rail with 2% tolerance, for example, is difficult on all oscilloscopes. This guide describes five tips for making accurate power integrity measurements with oscilloscopes.

TIP 1: ADJUST VIEWING CHARACTERISTICS



Waveform intensity

DC rail tolerance measurements require finding worst-case peak-to-peak voltage measurements (Vpp). This is best accomplished using an automated measurement. In addition, it is sometimes useful to get visual confirmation. All oscilloscopes have a display setting that allows the user to vary waveform intensity. This is typically set at about 50%. Adjusting to a higher level lets users more easily see oscilloscope pixels that the waveform crosses less frequently. The downside of turning up waveform intensity is that it makes it more difficult to tell how often any given pixel was illuminated. While important for viewing modulated signals, this distinction is generally not important for power integrity measurements.

Infinite persistence

Turn on infinite persistence and let the waveform build up across sequential acquisitions. Infinite persistence views can also be useful for documentation. The oscilloscope shows the range of DC voltage tolerance over a longer period of time.

Color grading

Turning on color grading creates more of a three-dimensional view of the power rail. Color grading combined with infinite persistence creates an insightful view of power rails signals.

TIP 2: LOWER NOISE

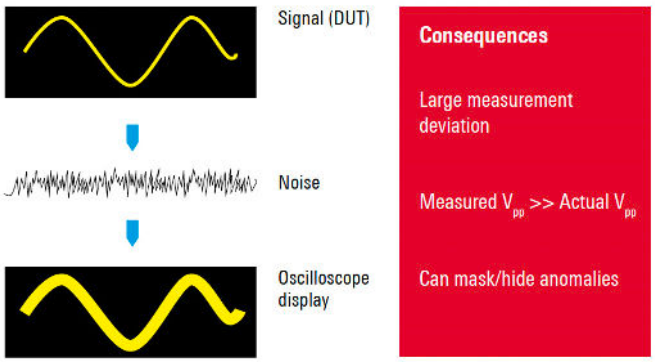
Choose an oscilloscope that has low noise

You will never be able to measure signals that are smaller than the noise of your oscilloscope and probing/cabling system. When a signal enters the oscilloscope, front-end noise gets added to the signal before the analog-to-digital converter (ADC). Each stored sample now includes the value of the original signal, but with some offset based on how much noise was present when the sample was acquired. Users will see this on the oscilloscope's display as thick waveforms, not to be confused with fast update rate. Peak-to-peak voltage values greater than what the true signal values are will be shown and measured.

The best approach is to start with an oscilloscope that has lower noise than other oscilloscopes. How do you determine how much noise an oscilloscope has? Most oscilloscope manufacturers will have a data sheet with typical RMS noise values for a specific oscilloscope, and these values will have been characterized across a large sample of oscilloscopes. Noise is a characteristic and not a specification. Moreover, manufacturers typically only publish RMS noise value, but peak-to-peak noise values are really what matters for accurate ripple measurements.

A simple method is to do a check yourself. A quick characterization takes just a couple minutes and requires no external equipment. Disconnect all inputs from the front of the oscilloscope, turn on a V_{pp} measurement, set the vertical scale and sample rate you are likely to use for your measurement and let the oscilloscope run until you have a stable and consistent V_{pp} noise value. Noise levels are dependent on the vertical sensitivity setting, the bandwidth setting and the path selection (50 Ω or 1 MΩ) and will vary slightly from channel to channel on the same oscilloscope.

Oscilloscopes from different manufacturers will have noise levels that may vary as much as 100%. If you need to make precise ripple measurements, make sure you choose an oscilliscope that has low noise.



Noise is the primary source of DC rail ripple measurement inaccuracy.

Disconnect inputs, select vertical sensitivity, bandwidth, and do a quick V_{pp} noise characterization of your oscilloscope. Turning on infinite persistence makes it easier to see the noise envelope.

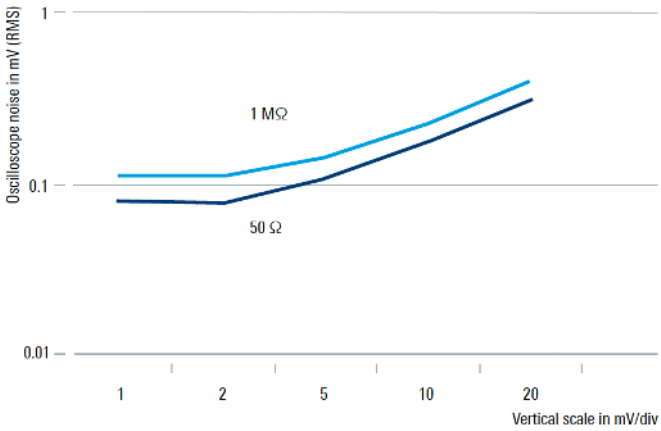
Choose the signal path that has the lowest noise

Oscilloscopes used for power integrity measurements commonly offer both 50 Ω and 1 MΩ signal paths. Users may have a probe that requires one of these paths, or may have a cabled power rail measurement.

The 50 Ω path is typically the quietest for all oscilloscopes that have both paths and allows for full oscilloscope bandwidth. Noise on the 1 MΩ path may be two to three times the noise of the 50 Ω path, and typically bandwidth is limited to 500 MHz on the 1 MΩ path, making the 50 Ω path a better choice for power integrity measurements.

Power rail impedance is generally measured in the mΩ range. For cabled measurements without any probes, the 50 Ω path has 50 Ω DC input impedance and therefore cause some resistive loading, reducing power rail DC amplitude values. Using a specialized power rail probe, such as the R&S®RT-ZPR20 with 50 kΩ input impedance, minimizes this issue.

It is not wise to connect a 50 Ω cable, such as a 50 Ω pigtail coax, directly to the oscilloscope's 1 MΩ inputs due to reflections that will occur between the 1 MΩ and 50 Ω transmission line mismatch.

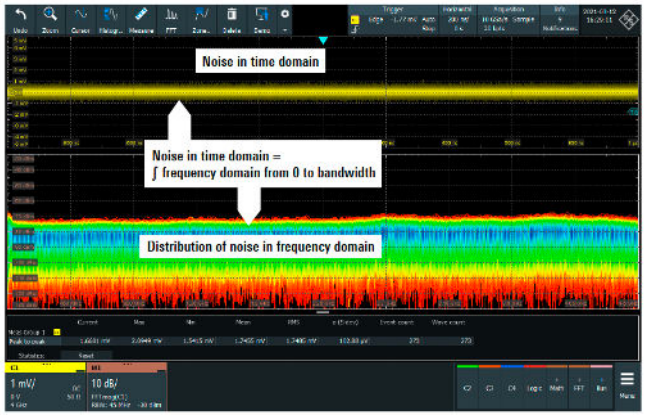


Comparison of noise on 50 Ω and 1 MΩ paths on the R&S®RTO oscilloscope at increasing vertical sensitivities.

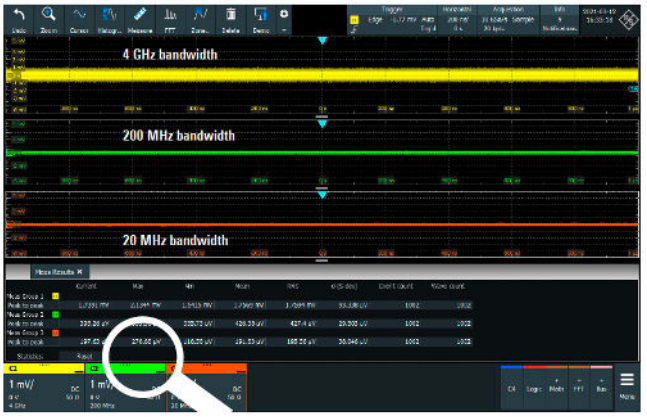
Use the most sensitive vertical scale

Noise is a function of full screen vertical value on the oscilloscope. So, using a more sensitive vertical resolution will reduce the amount of total noise measured. In addition, when you scale your signal to fill the majority of vertical space, the oscilloscope uses more of its ADC resolution and your V_{pp} measurements will be more accurate.

Noise is a function of vertical scaling. Choose the most sensitive vertical scale to reduce noise.In this example, 2 mV/div scales produces noise that is about 3 ½ times smaller than noise at 20 mV/div.



Do an FFT of your oscilloscope without any inputs connected, then compare with the FFT with signal connected. You will get a good feel for where signal content occurs and where higher frequency is just broadband noise from the oscilloscope and probing system. You can then set the bandwidth limit appropriately.



Bandwidth limiting reduces broadband noise, resulting in more accurate time domain measurements. With no inputs connected to oscilloscope channels, here's a comparison of noise at 1 mV/div at 20 MHz, 200 MHz and 4 GHz. 20 MHz V_{pp} noise is about 50% of noise at 200 MHz, and 13% of the amount of noise at full 4 GHz bandwidth.

Limit bandwidth

Noise is broadband. With no inputs connected to the oscilloscope, turn on an FFT and you'll see how much noise there is across the full bandwidth of the oscilloscope. Turning on bandwidth limit filters reduces broadband noise and will give you a more accurate power rail measurement. The tradeoff is that higher frequency anomalies won't show if bandwidth limiting is set too low.

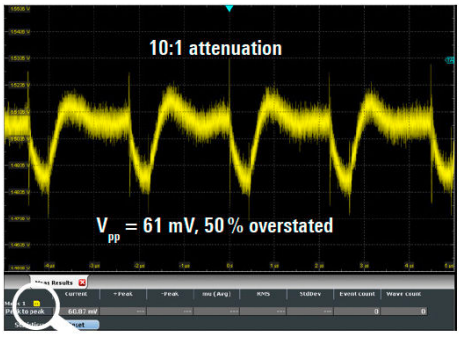
What is the right bandwidth to use? The answer is that it depends on your signals. While switching speed may be in the kHz range, fast edges produce harmonics that go into the MHz range. If you have higher frequency coupled signals, including clock harmonics, you will need more bandwidth to capture these. Both the R&S®RTO and R&S®RTE oscilloscopes come as standard with bandwidth limit filters. In addition, the HD mode option further reduces broadband noise and increases vertical resolution up to 16 bit.

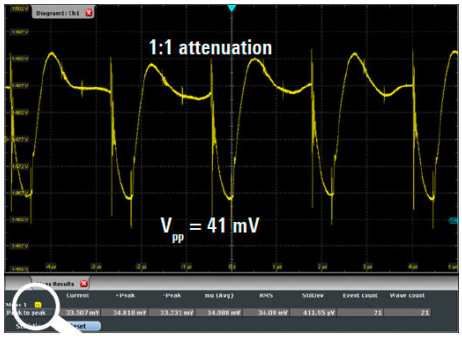
Choose the right probe (attenuation, bandwidth and connection)

Making accurate power integrity measurements can be greatly enhanced by using probes that have a 1:1 attenuation ratio. Probes that have higher attenuation ratios amplify noise. In addition, higher attenuation ratios limit vertical sensitivities that can be used. For example, a 1:1 probe on an oscilloscope with an input that goes down to 1 mV/div allows the user to scale at 1 mV/div, while a probe with a 10:1 attenuation ratio only allows users to scale down to 10 mV/div.

How you probe your power rail is as important as the other techniques we've talked about. Some users bring power rails out to SMA connectors where signal quality and accessibility is high. Other users choose to solder a connection. Still others will use a clip over a bypass capacitor as an easy access point. Others will probe using a handheld probe browser. Each technique has tradeoffs in terms of ease, required up-front planning and signal quality.

Using probes with 1:1 attenuation ratios for more accurate measurement results for small signals.





For highly accurate measurements, Rohde & Schwarz recommends the R&S®RT-ZPR20 power rail probe with a direct SMA or soldered 50 Ω SMA pigtail coax (included with the probe). This delivers extremely low noise with full 2 GHz bandwidth. While the probe is specified at 2.0 GHz bandwidth, its frequency response has a slow roll off and will capture 2.4 GHz Wi-Fi signals that may be coupled on the power rail. While 2.4 GHz amplitude values will be attenuated by about 3 dB, the ability to view these coupled signals can be important in finding coupled sources.

When using the R&S®RT-ZPR20 browser, R&S®RT-ZA25, bandwidth is reduced to 350 MHz. Using a ground that minimizes ground loop area, such as a ground spring, enables best measurement accuracy.

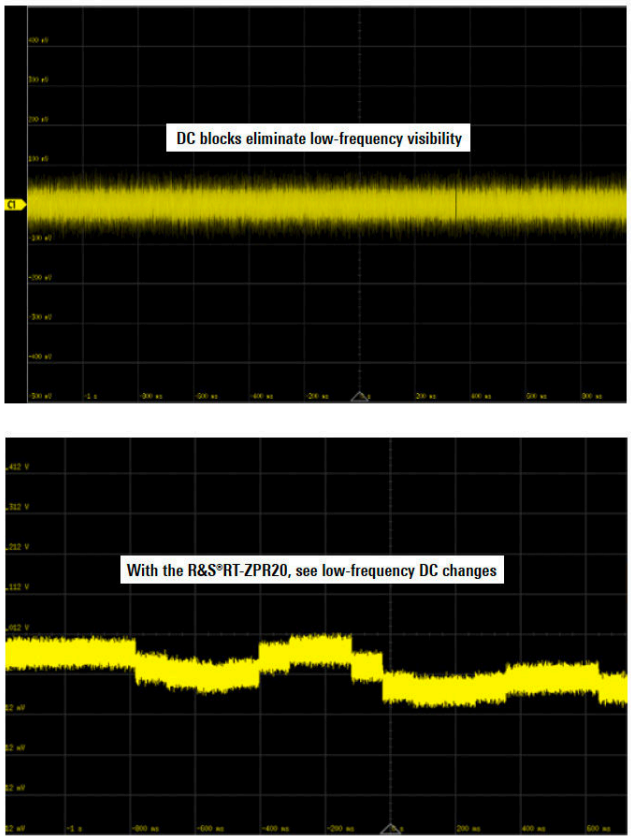
2 GHz coax solder in pigtail is shown connected to channel 2, while a passive 350 MHz browser with bypass cap clip and ground spring is shown to the right

TIP 3: ACHIEVE SUFFICIENT OFFSET

AC coupling and blocking caps

Scopes typically don't have sufficient built-in offset to allow users to place the waveform at the center of the display and zoom in. This results in two negative factors: the oscilloscope uses only a fraction of its ADC vertical resolution and uses a bigger vertical scale, causing additional noise. This makes for a low-quality measurement.

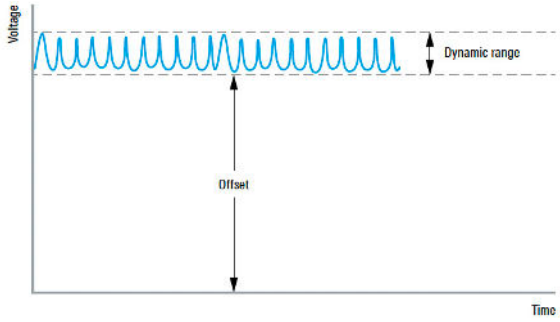
Blocking caps or using the AC coupling mode on the oscilloscope will remove the signal's DC component, if available for the selected path and probe. This solves part of the problem, but eliminates the ability to see true DC values and drift.



With a block cap or AC coupling, the oscilloscope does not see DC values or drift. With up to ±60 V built-in offset, even when zoomed with small vertical scaling, the R&S®RT-ZPR20 power rail probe enables users to see the absolute DC value including low-frequency DC changes.

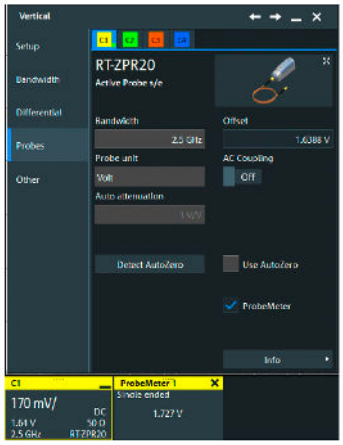
Probes with built-in offset

Some probes offer additional built-in offset. They have the advantage of allowing users to have sufficient offset to see true DC values and low-frequency characteristics such as drift and sag. For example, the R&S®RT-ZPR20 power rail probe has a built-in offset of ±60 V and a dynamic range of 850 mV. This means that users can look at AC characteristics up to 850 mV in height on DC rails anywhere between –60 V and +60 V.



R&S®RT-ZPR20 power rail probe with ±60 V built-in offset for zooming in on a wide range of DC power rail standards

The dynamic range specifies the maximum AC amplitude the probe will measure correctly. With a dynamic range of just 850 mV, the probe is really a specialized tool for measuring small AC perpetrations on DC rails. It is not a tool for measuring signals for other applications that require greater than 850 mV of AC amplitude.



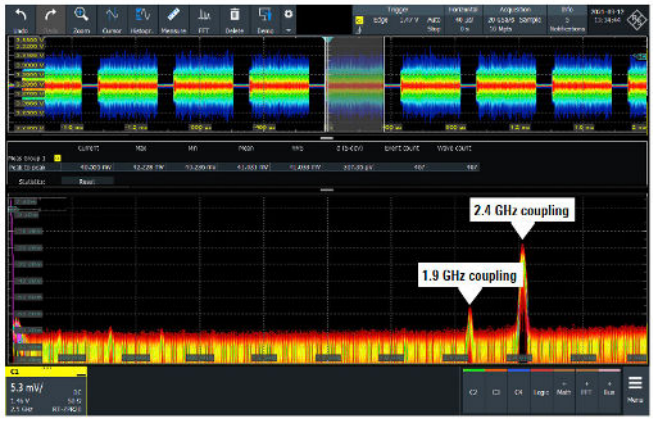
The R&S®RT-ZPR20 power rail probe includes an integrated R&S®ProbeMeter that shows the DC voltage, even if the signal is not on the oscilloscope display. This makes it easy to determine the required offset, or can simply be used to provide an accurate DC value.

TIP 4: EVALUATE SWITCHING AND EMI

Frequency domain view

Characterizing power rails typically involves ensuring there are no unwanted signals coupled onto the power rail. In addition, users sometimes need to look at switching harmonics. These are impossible to determine by looking at time domain waveforms, but are easy to see in the frequency domain using an oscilloscope's FFT.

How much bandwidth is needed for frequency domain views? It depends on the potential signals including clocks and fast edge harmonics that may be coupled onto the power rail.



Looking at the power rail in the time domain provides critical insight into V_{pp}. However, to find and isolate coupled signals on the power rail, such as this 2.4 GHz Wi-Fi signal, a frequency domain view is required. The R&S®RT-ZPR20 power rail probe has a specified bandwidth of 2 GHz and a typ. –3 dB bandwidth of 2.4 GHz. This allows users to still see coupled signals at 2.4 GHz.

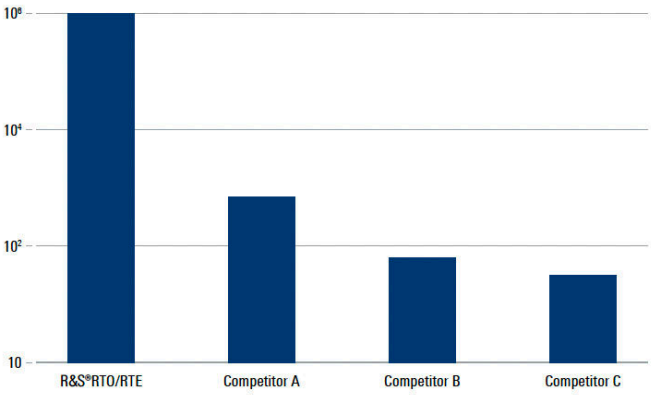
TIP 5: ACCELERATE MEASUREMENT TIME

Update rate impact on speed of power integrity measurements

Power rail measurements involve finding the worst-case amplitudes. Developing high confidence can mean taking hundreds or thousands of measurements across an extended window of time. This can take time, and can be tedious. Power integrity measurements are unique in that they often require large time spans. In order to retain higher bandwidth, the oscilloscope needs to maintain a faster sample rate, resulting in significant usage of memory.

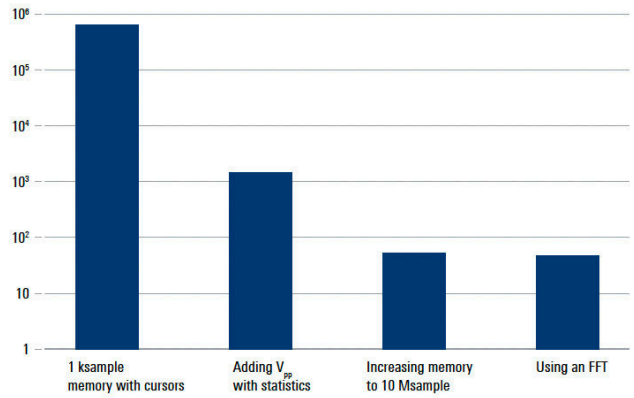
For example, capturing a millisecond at 10 Gsample/s results in a memory size of 10 Msample. Ten milliseconds capture results in 100 Msample memory usage.

Waveform update rate describes how fast the oscilloscope can process memory, show the result on the display and begin capturing a new acquisition. The R&S®RTO and R&S®RTE oscilloscopes for example have a maximum update rate of 1 million waveforms/s. Fast update rates mean that measurements such as V_{pp} and FFT will be done more quickly. Many oscilloscopes have a maximum update rate in the range of tens or hundreds of acquisitions per second. This means gaining confidence in finding worst-case tolerance violations will take orders of magnitude longer than an oscilliscope with fast update rate. Having an oscilloscope with fast update rate enables users to gain confidence more quickly.



Comparison of the R&S®RTO and R&S®RTE update rate with other oscilloscopes in the industry (log scale)

Best shown using a log scale due to the difference, the R&S®RTO and R&S®RTE have significantly faster update rates of up to 1 million waveforms/s in normal mode, the fastest in the industry. Both also have hardware-accelerated FFT. This performance advantage delivers faster power rail testing results.



Impact of measurements, memory depth increases, and the use of an FFT on the update rate of the R&S®RTO oscilloscopes (log scale)

The R&S®RTO and R&S®RTE maintain faster update rates than other oscilloscopes in the industry, resulting in quicker characterization of power rails.

SUMMARY

This guide covers five tips for making accurate power integrity measurements with oscilloscopes:

► Choosing an oscilliscope with low noise is critical to accurate power integrity measurements
► Coupling the oscilloscope with a 1:1 probe with built-in offset, high bandwidth, high DC impedance and an integrated R&S®ProbeMeter delivers superior capability and measurements
► Understanding and correctly setting a number of oscilloscope attributes such as vertical scaling and bandwidth limit filters increases the accuracy of results
► Adding frequency domain view enables users to quickly isolate coupled signals
► Fast update rates let users test power rails more quickly

When coupled with the R&S®RT-ZPR20 power rail probe, the R&S®RTO and R&S®RTE oscilloscopes give you faster, highly accurate power integrity measurements.

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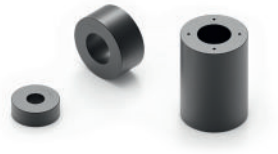

GOOD SI, PI AND EMC REQUIRE THIS MOST OF ALL...

Keith Armstrong
EMC Standards

Good SI, PI and EMC require a proper, grown-up understanding of electricity…Instead of what circuit designers are taught!

As electronic designers, we were taught the *children's version of electricity* at school, college, university, etc. This is the version that pretends (just as the SPICE simulator does) that electricity flows as little packets of charge totally inside conductors.

And we were taught that only the signals' send paths mattered. If we even thought about *return* paths at all, we just assumed they sort of happened somehow, and they couldn't be very important because our circuit design textbooks barely mentioned them. Even now, our circuit diagrams (schematics) only show send paths!

If we took a course on Maxwell's Equations, we learned lots of exotic maths, but nothing about how it related to actually designing electrical or electronic products, equipment, systems, etc.

And if we took a course on RF design, we learned all about designing with matched-impedance transmission lines – S parameters, Smith charts, and all that – but learned nothing about the RF behavior of send/return conductors that were not matched transmission lines even though these are the majority, in most applications.

If we took a course on RF Antenna design, we learned all about designing antennas for specific radio, TV, radar, etc. applications and services – but learned nothing about the antenna-mode behavior of *all other conductors* (which are the vast majority, in most applications).

We now need a proper understanding of electricity!

2.5GHz wireless datacomm's are ubiquitous and becoming inadequate; even the smallest cheapest microprocessors use clocks and signals with bandwidths of several GHz whether we need such high frequencies or not, and 5G cellular communications will use the spectrum between 18GHz and 100GHz to handle near-future datacomm's needs. The useful radio spectrum is now considered to extend up to 3THz (i.e. 3,000 GHz), which we will be using in the fullness of time.

Pretending that electricity flows as little packets of charge totally inside conductors does not allow us to design modern electronic technologies so that they even function correctly (SI and PI issues), never mind have good EMC.

So: here's a very brief overview of a proper understanding of electricity

I will expand on each of these issues, with practical examples, in future blogs

1. All electrical signals, data, power, wireless datacomm's and broadcasting, radar, etc., are really electromagnetic (EM) waves that propagate at the 'speed of light'.

2. The 'speed of light' is lower in all materials other than air or vacuum. This means that – at any given frequency – the EM waves propagating in such materials have shorter wavelengths than they would have if they were in air or vacuum.

3. We generate and receive EM waves (which we call signals, data, control, power, radio, TV, radar, etc.) using two conductors, usually identified on a circuit diagram as send and return.

4. Stray (leaked, parasitic, sneak, coupled, etc.) waves and currents always occur, but their send and return current paths may not be obvious. Despite the fact that they cause many EMI problems, we never show them on our circuit diagrams.

5. When we are more concerned with the patterns that EM waves make in 3-D space than in their propagation, we call the patterns 'EM fields'.

6. All currents – whether signals, data, control, power, etc. – always flow in closed loops. This includes all stray (leaked, parasitic, sneak, coupled, etc.) currents, too.

7. All currents preferentially flow in the loops with the lowest overall impedance. These current loops are not limited to the conductors we draw in our circuit diagrams – they can include displacement currents (i.e. electric flux coupling) and/or magnetic flux coupling through the air and other insulators.

8. All currents flowing in conductors flow closer to their outer surfaces as the frequency increases. This is called the Skin Effect, and it is the reason why we can use conductors as EM shields. However, conductors don't care what names we call them, so all conductors – whatever their function in our circuits, even signal or power wires and PCB traces – have skin effect whether we want them to or not.

9. There is a perfect correlation between a conductor's surface currents and the EM fields in the insulating media around the conductor (usually PVC, or air). We can say that the surface currents create the near-fields, or that the near-fields create the surface currents – either/both statements are equally true. So, we can choose to visualize/work with either the surface currents or the near fields – whichever is most appropriate for the issue we are dealing with.

10. All conductors have series impedances for AC currents, even superconductors with absolutely zero series resistance. So, whenever two or more circuits share any conductor – for example, those we might call earth, ground, chassis, 0V, DC power rail, live, phase, neutral, etc. – these series impedances cause noise to couple between them. Calling a conductor 'earth', 'ground', 'chassis', etc. does not endow it with magical properties! When an AC current flows in it, an AC noise voltage inevitably arises. This is called common impedance coupling, and it always happens because everything has impedance.

11. The EM waves propagating along their intended conductors have both electrical and magnetic field components (it's where the word 'electromagnetic' comes from).

12. They spread around in the space around the send/return conductors, depending on the physical arrangement of those conductors (closer send/return conductor spacing generally creates more compact fields). Other conductors exposed to these electric and magnetic fields pick up a proportion of them, and suffer noise as a result, Crosstalk is a typical example of such noise coupling.

13. EM waves in the air or other insulators have 'wave impedance': the ratio of their electric to magnetic fields.

14. Send and return conductors have 'characteristic impedance': the square root of the ratio of their mutual inductance to their capacitance, per-unit-length.

15. Changes in wave or characteristic impedances reflect some of the propagating EM waves in the air or in conductors respectively, causing signal integrity (SI) and power integrity (PI) problems in circuits, and causing resonances in conductor structures. These reflections make every pair of send/return conductors (including those carrying stray currents), into 'accidental transmitting/receiving radio antennas'. (Note that send/return conductors that are carefully designed as 'matched transmission lines' along their entire length don't have significant impedance discontinuities, so help maintain good SI and PI, and are relatively ineffective as 'accidental antennas'.)

16. Resonating send/return conductors can have impedances between very low indeed (μW) and very high indeed (hundreds of kW or more). This means that even very low-resistance conductor pairs (such as thick bars of copper) can behave almost as open-circuits at certain frequencies, depending on their dimensions.

17. Conductive structures such as planes and enclosures can experience 'accidental' structural resonances, which makes them behave as various types of 'accidental' antennas. The magnetrons in microwave cookers are an example of intentionally designing a metal enclosure (a cavity) as a resonant antenna, to help couple energy into food (in this application).

18. All 2-dimensional and 3-dimensional conductive structures behave as accidental antennas due to the shapes and dimensions of their structures, and at frequencies where their shapes and dimensions are comparable with wavelengths – they can resonate. The lower the resistance of the conductive parts forming the structure, the higher the 'Q' at such resonances. So, at these structural resonances, sturdy metal structures with very low resistances in their parts can suffer overall impedances that can be very low indeed (even μOhms), or very high indeed (even hundreds of kOhms or more). This is true whether we call these structures 'ground', 'earth', 'chassis', shield, frame, 0V, etc.

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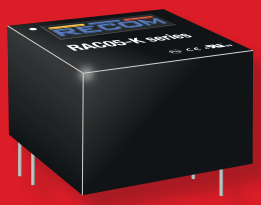
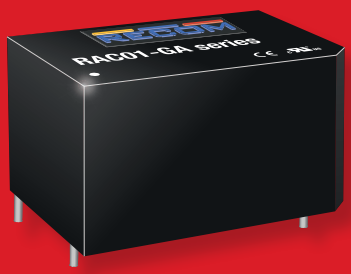
- No external components needed
- Standby mode optimized PSU (ENER Lot 6)
- Fully protected (SCP, OCP, OVP)
- UL/IEC/EN certified 60950, 62368, 60335
- Suitable for industry 4.0, IoT, building automation and household applications





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SIGNAL INTEGRITY ALONG PCB TRACKS

Steve Roberts
Innovation Manager, RECOM Power GmbH

The most common conductor used in electronic circuits is copper. The Direct Current (DC) resistance of Printed Circuit Board (PCB) tracks depends on their cross-sectional area and length and can be calculated using the following formula:

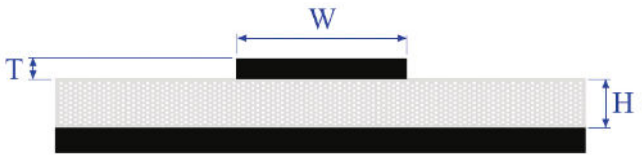
$$Track\ Resistance = \frac{Length}{Thickness\ x\ Width}.Resitivity\ of\ copper$$

Eq. 1: Copper track DC resistance

A typical PCB has a copper thickness of 35µm (1.37 mil), so a trace 1mm wide and 1cm long will have a DC resistance of nearly 5mΩ at 25°C, increasing to 6mΩ at +85°C. (copper resistivity is $1.7x10^{-6}$ Ω/cm and its temperature coefficient is +0.393%/°C).

In addition to the DC resistance, the Alternating Current (AC) track impedance must also be considered. A PCB track has both an inherent inductance and a distributed capacitance which means that the basic DC resistance needs to be modified to an AC impedance which is frequency dependent. The track impedance can lead to unexpected results as signals are capacitively or inductively coupled between tracks, copper planes and other components.

For example, a top PCB track passing over another track on the PCB bottom (or within the PCB if it is multilayer) will have a characteristic impedance, Z_0, and a track characteristic capacitance, C_0, according to the following relationship:



$$Characteristic\ Impedance, Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{0.98H}{0.8W + T}\right)\ Ohms$$

$$Characteristic\ Capacitance, C_0 = \frac{0.67(\varepsilon_r + 1.41)}{\ln(\frac{5.98H}{0.8W + T})}\ pf/inch$$

Eq. 2: Characteristics relationships for copper PCB track with a ground plane

For a typical PCB, ε_r = 4, H = 30mil (0.76mm) and T = 1.37mil (35µm), so a 1mm wide track will have a characteristic impedance, Z_0, of around 65 Ohms and a characteristic capacitance of around 82pF/m.

Therefore, it is important that PCB tracks do not pass over or close to other signal tracks. Ideally, a double-sided or multilayer layout should be used so that a ground plane can placed underneath tracks carrying high frequency signals. If the PCB is only single sided, then the power connections should be kept as short and as wide as possible with sufficient separation to signal-carrying tracks.

Furthermore, the characteristic impedance and capacitance will affect the integrity of the signals carried by the copper conductor.

Firstly, there will be a delay in the propagation of the signal equal to the characteristic capacitance, C_0, multiplied by the characteristic impedance Z_0, expressed as picoseconds/inch.

$$Propagation\ Delay, T_p = C_0 Z_0\ psec/inch$$

Secondly, if we inject a square wave (e.g., a clock signal) into a long track, then the waveform at the end of the track will not be the same as the original. The distributed parasitic inductances and capacitances will create a transmission line which will distort the signal depending

on the impedances of the source, load and track in between. *Figure 1* below shows a typical result for a long trace and a clock signal with fast slew rates:

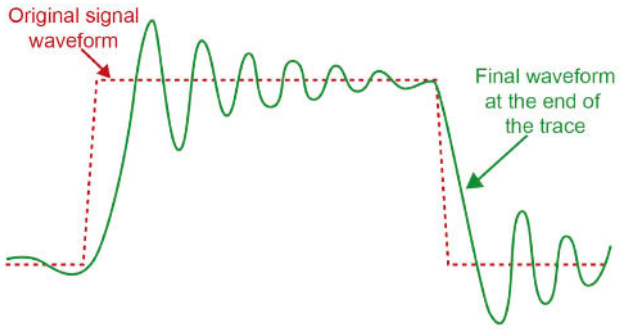


Fig. 1: Effect of PCB track characteristic impedance on high frequency signals

Many engineers and circuit designers refer to this overshoot/undershoot effect as "ringing" and it is a cause of electrical overstress damage to many kinds of components as the peak positive and negative voltages can exceed the maximum limits of the components.

For Electro-Magnetic Compatibility (EMC), such ringing also generates radiated emissions as the clean square-wave pulse or clock signal generates high frequency oscillations that lose some of their energy by radiating it out to their surroundings – in effect, the simple PCB trace has turned into an accidental radio antenna (black trace in the diagram):

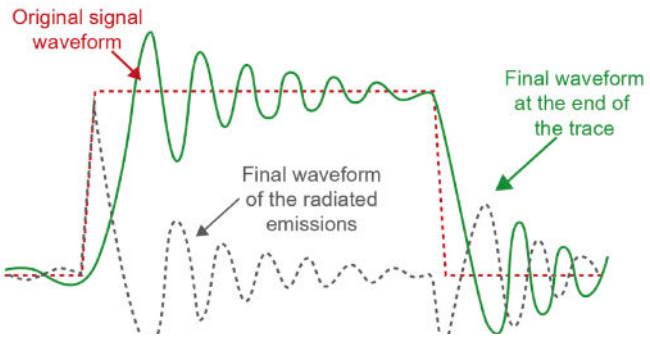


Fig. 2: Radiated emissions caused by high frequency signal ringing

This radiated energy occurs over a range of frequencies over a wide spectrum that is much higher than the original frequency of the signal waveform.

This is as good a point as any to introduce the concept of spectra and Fourier analysis.

Fourier Transform

Joseph Fourier (1768-1830) determined that any periodic signal can be represented by the sum of a series of sinusoidal signals of various frequency, phase and amplitude (the Fourier Series). The Fourier Transform shifts information from the time domain to the frequency domain (and vice versa). The result of a Fourier Transform on a periodic signal is the equivalent Fourier Series or spectrum.

The figure below shows graphically the first six harmonics, or equivalent component sinusoidal signals, of a square wave. If all these harmonics are added together, the result will be the red summed series waveform shown at the front of the diagram. The more harmonics that are included, the closer the summed waveform will be to the original square wave.

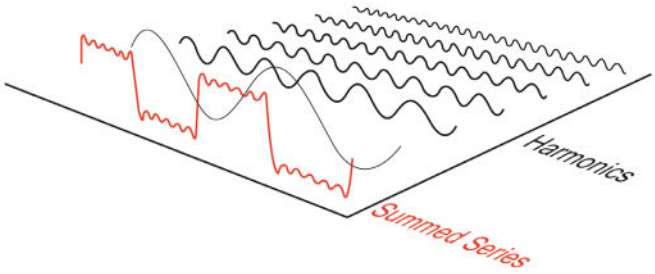


Fig. 3: Fourier Series (from DC/DC Book of Knowledge Fig. 2.12)

Fourier demonstrated that any continuous periodic waveform can be represented by a sum of a series of sine waves of various frequencies and signal strengths:

$$x(t) = \sum_{n=-\infty}^{\infty} \left(c_n e^{j\omega_0 n t}\right)$$

Eq. 3: Fourier series representation

where the signal x(t) is represented by the sum of *n* individual sine waves, where C_n is the *n*th coefficient (amplitude) with ω_0 being the first harmonic in radians ($=2\pi f_0$), n being the *n*th harmonic frequency and t being time. *n* = 0,1,2,3,…..

Thus, a Fourier transform takes any periodic waveform and generates a spectra of individual sine waves that in sum represent that waveform.

The Fourier transform is a very useful tool to convert complex waveforms into their component spectrum of frequencies. What makes Fourier transforms so powerful and useful is that it allows us to identify precisely the frequencies that are causing the unwanted interference, allowing us to design the most appropriate filter or to reassess the PCB layout or grounding to eliminate the noise source or the characteristic that is distorting the signal.

For example, applied to the radiated emissions from the long PCB trace, we get a radiated spectrum of harmonic frequencies:

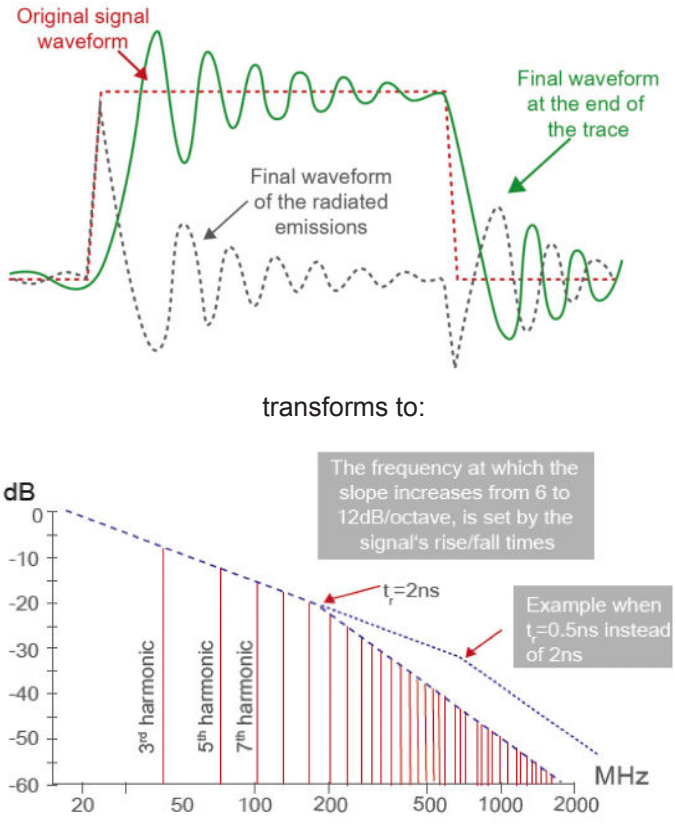


Fig. 4: Fourier Transform

A 16 MHz clock signal sent along a long PCB trace can create an unintentional antenna with a radiated harmonic emission spectrum continuing up to nearly 2 GHz. Even a 50 kHz PWM switch-mode power supply can easily generate harmonic frequencies ranging up to 50 MHz.

Vias

It is not just long PCB traces that can cause unwanted oscillations, PCB vias (the vertical connections between tracks) are often the cause of significant parasitics, both a parasitic inductance, L, and a parasitic Capacitance, C, which are both dependent on the geometry of the via:

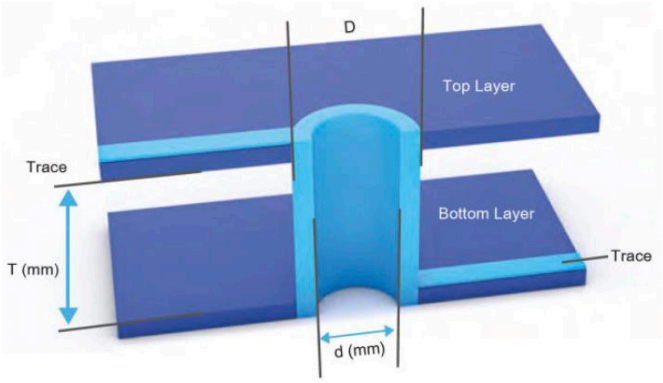


Fig. 5. Via dimensions

$$Via\ Inductance, L \approx 5.08T\left[\ln\left(\frac{4T}{D}\right)+1\right] \text{nH}$$

$$Via\ Capacitance, C \approx \frac{0.25TD}{D-d}\ pF$$

$$Via\ Characteristic\ impedance, Z_0 = 31.6\sqrt{\frac{L(nH)}{C(pF)}}\ Ohms$$

Eq. 4: Via parasitics

Where T is the board thickness, D is the diameter of the pad surrounding the Via and d is the via clearance hole diameter, and assuming bulk permittivity (εr) is 4.5 for FR4 boards.

A typical 0.4mm (0.016") Via through a 1.6mm (0.063") PCB will have a parasitic inductance of around 1.2nH and a parasitic capacitance of 0.33-0.4pF, rising to about 0.8pF when the via pads and track connections are considered.

As with the PCB tracks, these parasitics will have a characteristic impedance which will cause a signal transmission delay:

$$Via\ Propagation\ Delay, T_p \approx 80\sqrt{L(nH)C(pF)}\ ps/inch$$

These parasitic elements of PCB pads, tracks and vias adds significant complexity to the layout, as this example for a simple op-amp circuit shows:

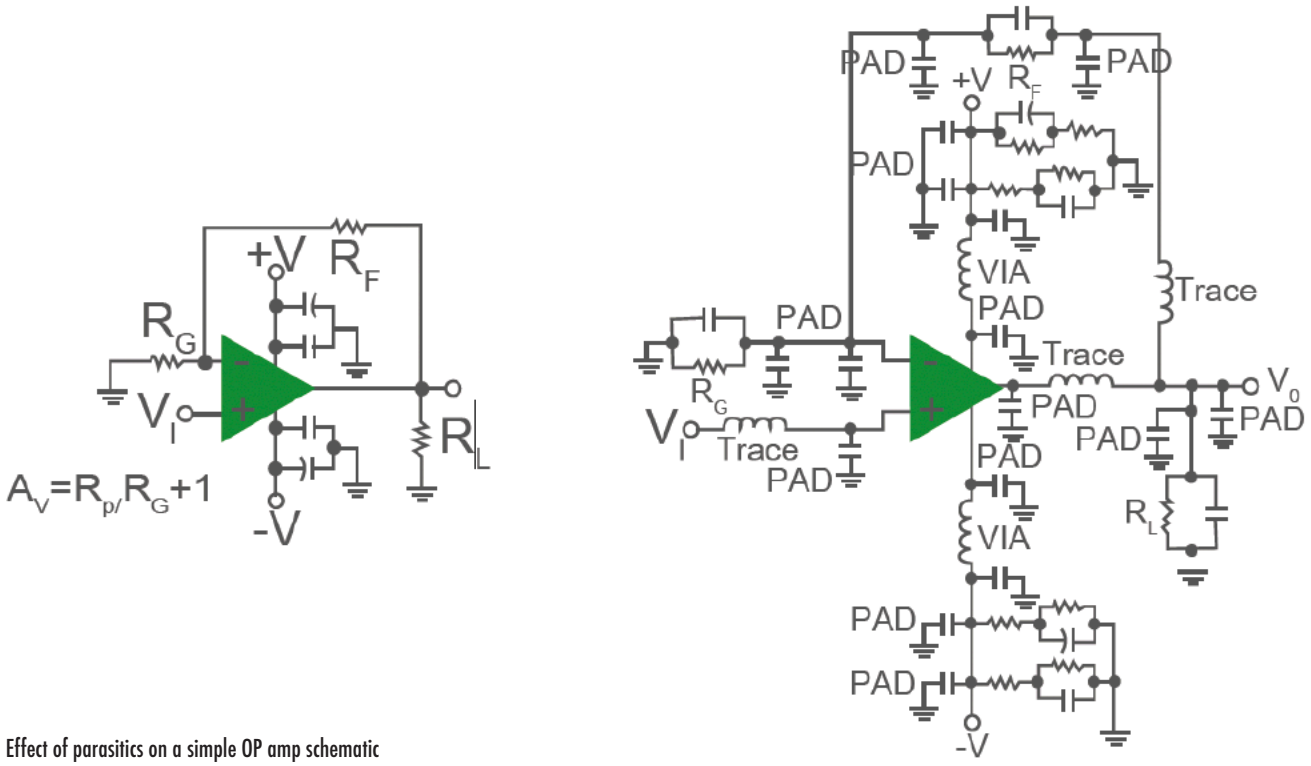


Fig. 6: Effect of parasitics on a simple OP amp schematic

Countermeasures – Controlling Track Impedances

The overall impedance of via connections between tracks can be reduced by placing several vias in parallel, with the disadvantage that the stray capacitance increases.

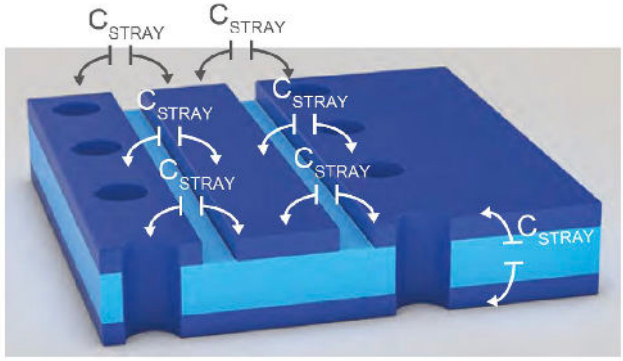
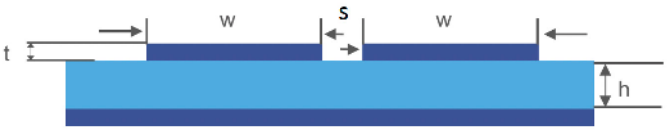


Fig 7: Using multiple vias to reduce overall impedance at the cost of increased stray capacitance

For high speed track connections, PCB track impedance matching between source and sink will reduce reflections and therefore radiated emissions.

The characteristic impedance is dependent on the layout dimensions, so a PCB transmission line can be created by choosing the appropriate track thicknesses and separations.



As in Eq.2, the characteristic impedance for single-ended signals can be calculated from:

$$Single-Ended\ Impedance, Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98H}{0.8w + t}\right)\ Ohms$$

but the edge-coupled strips have a differential impedance when used with differential signals:

$$Differential\ Impedance, Z_d = 2Z_0\left[1 - 0.48^{\left(-0.96\frac{s}{h}\right)}\right]\ Ohms$$

Fig 6.8: Microstrip dimensions and characteristic impedances

For example, two PCB tracks with a characteristic impedance of 50 Ohms placed with a separation of 1mm (40 mils) on a PCB thickness of 0.76mm (30mils) will have a differential impedance of around 86.6 Ohms.

As a rule-of-thumb, if the trace is longer than ¼ of the distance travelled during the rise time of the signal, then a transmission line approach is required.

For example, if we have a signal with a 0.5ns rise time, then:

$$Propagation\ velocity, v = \frac{c}{\sqrt{\varepsilon_r}} \approx \frac{3.10^{10}}{\sqrt{4}} \approx 15cm/ns$$

The distance travelled during the rise time will be about 15/0.5ns = 7.5cm, so the critical PCB track length will be a quarter of that, or 1.875cm.

Different high speed interface signals have different target impedance tolerances which need to be addressed to maintain signal integrity.

Signal	Target Impedance	Tolerance
USB 2.0	90 Ohms	±10%
USB 3.1	90 Ohms	±5%
HDMI	95 Ohms	±15%
Ethernet Cat.5	100 Ohms	±5%
DisplayPort	100 Ohms	±20%

Target impedances are also relevant for board level power distribution. With many FPGA and ASICs running on 1V or less supply rails, any oscillation on the supply rails due to current peaks could create an out-of-range supply voltage.

The target characteristic impedance can be calculated from:

$$Z_{0,target} = \frac{V_{supply} \cdot V_{ripple}(\%)}{50\%. I_{peak}}$$

V_{ripple} (%) is the maximum allowed deviation in the supply voltage (voltage regulation + transients).

Conclusion

Maintaining signal integrity on a PCB needs careful layouting and separation of power and signals.

Although the majority of the effects of track impedances, parasitics and capacitive coupling only become significant at high frequencies, the spectra of signal harmonics can extend up into the Megahertz region and beyond, often causing unanticipated signal integrity problems even for relatively low frequency signals.

Understanding how signals propagate along PCB tracks and through Vias will help mitigate these issues.

POWER INTEGRITY OVERVIEW FOR PCB DESIGNERS

Zachariah Peterson
Technical Consultant, Altium

Most PCB designers don't realize they have a power integrity problem until that problem causes a board to fail. Power integrity is also related to two other important areas that repeatedly cause design failures: signal integrity and EMI/EMC. In fact, some common signal integrity problems are related to power integrity in that unstable power leads to signal level and timing fluctuations. In addition, some EMI problems can be caused by excessive emissions by fast transients within a power system.

To help PCB designers and systems engineers better overcome their power integrity problems, it's important first to know how power integrity can cause other problems in a circuit board. This article will give an overview of the power integrity problems more designers are experiencing in modern electronics systems and which will become more prevalent as devices reach greater feature density in the near future.

Who Worries About Power Integrity?

Generally, when we refer to power integrity, we refer to AC power integrity, meaning time-varying changes in the power being delivered to a load. DC power integrity is also important, but is more the domain of power electronics rather than high-speed digital systems.

The goal in designing for stable power integrity is to minimize power fluctuations in a PCB as components pull power from the power distribution network (PDN). The typical area where power integrity is important is in boards with many high-speed components, although to an extent the same challenge arises in high-frequency systems. The reason power integrity arises so often in this system is due to the fast edge rates of digital signals; generally any digital system with fast GPIOs, fast SPI buses, and standardized computing peripherals can have power integrity problems.

The result of such power rail and ground plane potential fluctuations includes signal integrity and EMI problems such as:

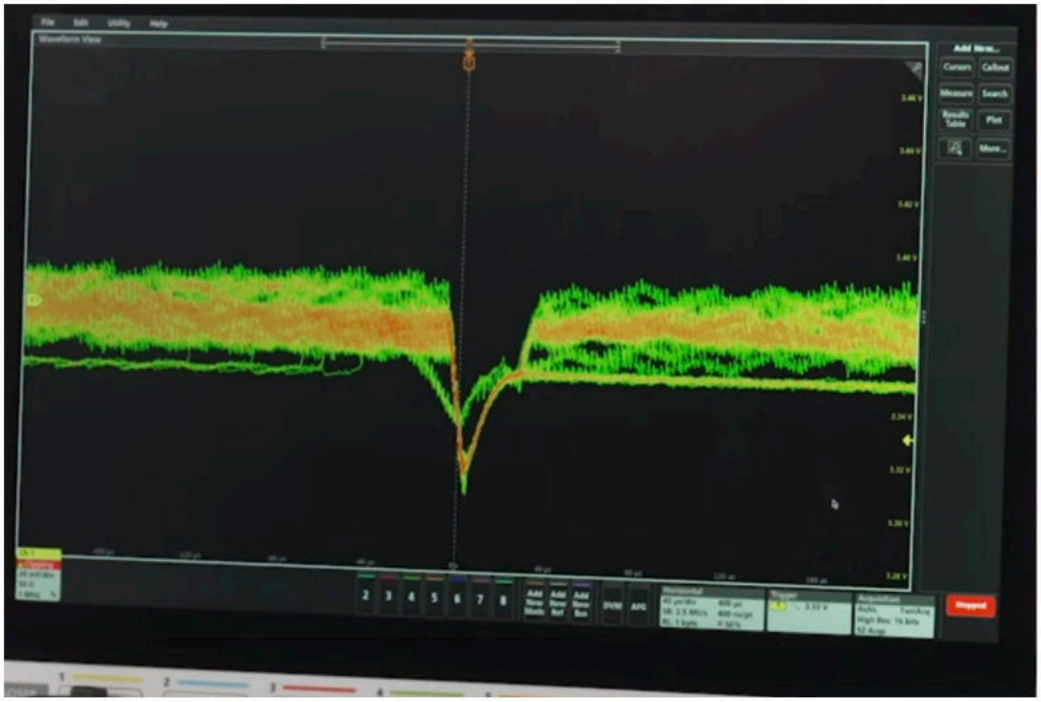
- Transient ringing seen on I/O signal levels
- Jitter, observed in edge transitions in an eye diagram
- Radiated emissions, which may be observed from the surface or board edge
- Noise transfer between poorly isolated rails with the same voltage

These problems can occur despite precise design and layout of power regulator circuits. Of course, power regulators have their own noise challenges, but the noise observed on a power rail in a high-speed PCB is really a low-impedance power delivery challenge, not a regulator noise challenge.

Observing Power Integrity

The effects of power integrity on power delivery can be measured directly by looking at the voltage provided by a PDN in a PCB. Power is delivered to components by first charging up the capacitance in the PDN; the PDN then discharges some current through the I/O supply when logic outputs switch states. Because modern CMOS-based I/O buffers switch very quickly, they excite a broadband transient in the PDN that exhibits an underdamped oscillation in system voltage level.

Power delivery instabilities can be seen in an oscilloscope trace. The image below shows just such a power droop event occuring at the moment a certain IC switches its logic state with fast edge rate. The resulting voltage dropout in the rail is significant and ends with an underdamped oscillation. If this dropout is too large, it could exceed the lower power limit of components that are drawing power from the PDN, causing system resets.



Significant power droop observed on a 3V3 rail in a single-board computer.

With further probing throughout the PCB, it is possible to identify specific components that may have insufficient decoupling/bypassing and investigate how these are placed in the PCB. The other factor contributing to unstable power delivery is the layer stackup in the PCB. Potential changes to a design can be qualified in simulation to determine their efficacy.

Designing PDN Impedance

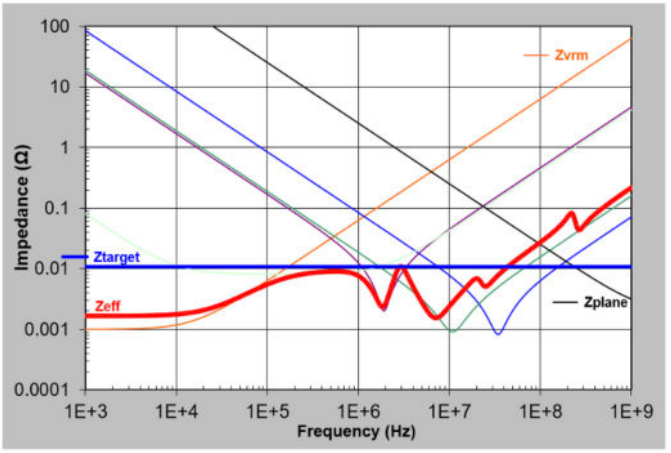
The impedance of the PDN in a PCB is actually a matrix, with its members being self-impedances for each power rail and transfer impedances between power rails. The typical concern in designing the PDN for large processors requiring multiple rails is to ensure the self-impedance for each rail is minimized throughout some relevant bandwidth (typically extending up to GHz frequencies).

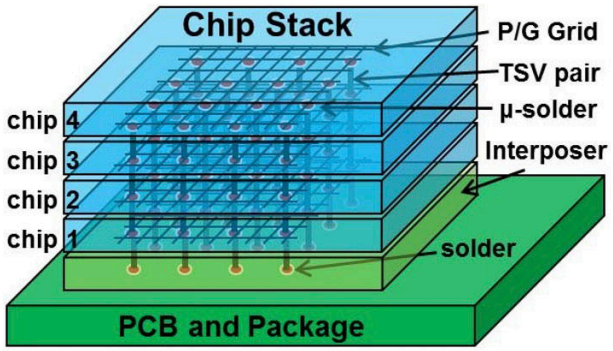
In starting the PDN design process, the designer first needs to formulate two metrics:

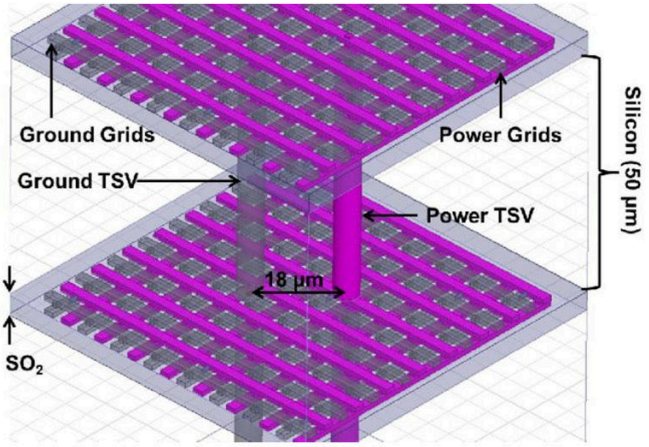
- An acceptable voltage ripple range based on noise margin
- A target impedance based on the expected maximum average current draw and allowed voltage ripple

As core voltages have decreased, being as low as 0.8 V in some components, the noise margin compresses and this creates greater pressure on the PCB designer to ensure lower PDN impedance.

An example PDN impedance spectrum with 1 mΩ target impedance is shown below. In this example, we can see each of the contributors in the PCB layout to the overall impedance (VRM, plane, and groups of decoupling capacitors). This model was generated analytically by considering the equivalent circuit parameters of the structures that make up a PDN in a PCB (planes, vias, traces, capacitor parasitics,VRM model). A more accurate PDN impedance spectrum could be generated using a full-wave solver.







Transfer impedance is used to evaluate isolation between different rails, where the focus is on evaluating how current draw at one port produces a voltage fluctuation at all other ports. This takes a design-simulate-optimize strategy at the circuit level, which can be done in SPICE. This would later be verified in the PCB layout with a full-wave solver, producing an impedance curve similar to the example shown on page 22.

At the system level, we must also consider the on-die PDN impedance, as well as any in-package capacitance used to keep the on-die impedance low. Semiconductor packages can have highly inductive PDN impedance at GHz frequencies, which leads to a large peak (strong antiresonance) in the PDN impedance spectrum. In some cases, the best the PCB designer could do was load up on small-case decoupling capacitors and excess plane capacitance through the stackup design methods shown above.

Modern semiconductor packages, including multi-chip modules and 2.5D/3D integrated packages, could include additional in-package capacitance to ensure lower PDN impedance in the GHz range in order to ensure stable power delivery. An example low-impedance package design methodology involving formation of grounded grids surrounding through-silicon vias in a 3D package is shown above.

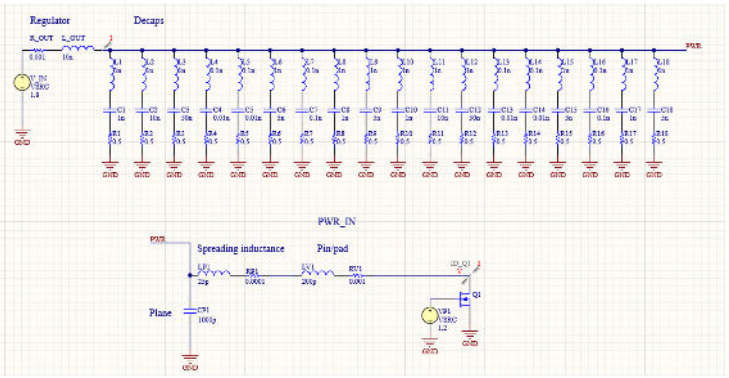
Simulating Power Integrity

The board used to gather the image shown above was built with best practices in terms of its stackup (adjacent power/ground planes), but still the droop arises due to insufficient capacitance in the PDN. These dropout events are difficult to predict during the design phase as they require sophisticated simulations:

- Pre-layout simulations using SPICE-based models
- Post-layout simulations using full-wave electromagnetic field solvers

SPICE-based models have always been phenomenological, although they are effective for evaluating components selection and isolation between power rails. Some of the best EDA vendor tools are now reaching the point where reduced full-wave simulations can be performed directly from PCB layout data to evaluate signal integrity.

The primary quantity to simulate when designing a PCB for stable power integrity is the PDN impedance. This would typically be generated in the frequency domain using S-parameters or transfer functions, or it could be examined in the time domain, where the voltage transient on a power rail is used to determine the PDN's impulse response function. In either case, the goal is to examine the impedance of the PDN given a proposed stackup and known decoupling capacitor counts.



Example SPICE model generated in Altium Designer. This model includes a decoupling capacitor bank, equivalent circuits for planes, and a simple switch to simulate current draw by an integrated circuit.

#	Name	Material	Type	Thickness	Weight	Dk
	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask	0.8mil		3.5
1	L1 TOP		Signal	1.6mil	1oz	
	Dielectric 1	RO3003 core, 17um rolled copper	Core	5mil		3
2	L2 GND		Signal	0.8mil	1/2oz	
	Dielectric2	RO4450F	Prepreg	5mil		4.2
3	L3 SIGNAL 1		Signal	0.6mil	1/2oz	
	Dielectric3	RO4835 core, 17um "LoPro" copper	Core	10.7mil		3.66
4	L4 GND		Signal	0.6mil	1/2oz	
	Dielectric4	370HR	Prepreg	5mil		4.2
5	L5 SIGNAL 2		Signal	1.2mil	1/2oz	
	Dielectric5	370HR	Core	10mil		4.34
6	L6 SIGNAL 3		Signal	0.6mil	1/2oz	
	Dielectric6	370HR	Prepreg	5mil		4.2
7	L7 GND		Signal	0.8mil	1/2oz	
	Dielectric7	RO3003 core, 17um rolled copper	Core	5mil		3
8	L8 BOTTOM		Signal	1.6mil	1oz	
	Bottom Solder	Solder Resist	Solder Mask	0.8mil		3.5
	Bottom Overlay		Overlay			

This example stackup, generated in Altium Designer, uses hybrid construction to support both high speed digital signals and RF signals. Based on layer thicknesses and Dk values, an ideal place to put a power plane or large power rails would be on L5.

Stackup and Materials Matter

The best predictor of power integrity in a PCB is the design of the stackup. The reason we care about the stackup is because it enables inclusion of plane capacitance through placement of an adjacent power-ground plane pair. Modern processors operating with fast edge rates need to have a power-ground plane pair with high plane capacitance for two reasons:

1. To ensure low PDN impedance up to higher frequencies
2. To compensate for any lack of on-die/in-package capacitance

Ensuring high plane capacitance requires placing the two planes close together on a thin core or prepreg layer, and the separating dielectric must have high dielectric constant. Together, this provides sufficient capacitance and low spreading inductance which can cause the plane's impedance minimum to reach near the GHz range.

To aid power integrity in smaller devices that require significant power draw, some advanced materials vendors supply embedded capacitance materials. These materials are very thin, being designed to separate the power-ground plane pair in the layer stack. They also have high Dk value and high loss tangent in order to provide high capacitance and dampen any radiated emissions from the power-ground plane pair. These materials are used in high layer count rigid or flex PCBs in mobile devices, and in the newer substrate-like PCBs used in modern smartphones.

Summary

As more designers confront power integrity challenges in PCBs and packaging, EDA vendors have a role to play in providing tools to iterate designs without repeated prototyping. The next generation of tools is providing an in-app approach to design optimization without requiring an external simulation program, including in the area of signal and power integrity. As more simulation application vendors form partnerships with EDA/ECAD vendors, we can expect these tool sets to expand to give more designers advanced capabilities for design and simulation in the areas of power integrity, signal integrity, and EMI.

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