SPRING 2024
electronics-cooling.com

electronics COOLING

FEATURED IN THIS EDITION

KEEP IT COOL

- Thermally conductive adhesives
- Non-curing thermal compounds, greases, pastes & gels
- Dispensable thermal pads & tapes
- Liquid thermal encapsulants
- Dispensing equipment

ELLSWORTH ADHESIVES

CONTENTS

electronics COOLING
electronics-cooling.com

PUBLISHED BY
Lectrix
716 Dekalb Pike, #351
Blue Bell, PA 19422
Phone: +1 484-688-0300
info@lectrixgroup.com
lectrixgroup.com

CHIEF EXECUTIVE OFFICER
Graham Kilshaw | graham@lectrixgroup.com

DIRECTOR OF BUSINESS DEVELOPMENT
Ashlee Zapata-McCants | ashlee@lectrixgroup.com

CREATIVE DIRECTOR
Kate Teti | kate@lectrixgroup.com

GRAPHIC DESIGNER
Marcos Cruz | marcos@lectrixgroup.com

DELIVERY MANAGER
Mackenzie Mann | mackenzie@lectrixgroup.com

EDITORIAL BOARD

Victor Chiriac, PhD, ASME Fellow
Co-founder and Managing Partner
Global Cooling Technology Group
vchiriac@gctg-llc.com

Genevieve Martin
R&D Manager, Thermal & Mechanics Competence
Signify
gmartin.sig1@gmail.com

Alex Ockfen, P.E.
Manager, Thermal & Mechanical Simulation
Meta
alex.ockfen@fb.com

Ross Wilcoxon, Ph.D.
Senior Technical Fellow
Collins Aerospace
ross.wilcoxon@collins.com

►**SUBSCRIPTIONS ONLINE**
at electronics-cooling.com

For subscription changes email
info@electronics-cooling.com

All rights reserved. No part of this publication may be reproduced or transmitted in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, or stored in a retrieval system of any nature, without the prior written permission of the publishers (except in accordance with the Copyright Designs and Patents Act 1988).

The opinions expressed in the articles, letters and other contributions included in this publication are those of the authors and the publication of such articles, letters or other contributions does not necessarily imply that such opinions are those of the publisher. In addition, the publishers cannot accept any responsibility for any legal or other consequences which may arise directly or indirectly as a result of the use or adaptation of any of the material or information in this publication.

Electronics Cooling is a trademark of Mentor Graphics Corporation and its use is licensed to Lectrix. Lectrix is solely responsible for all content published, linked to, or otherwise presented in conjunction with the Electronics Cooling trademark.

FREE SUBSCRIPTIONS

Lectrix®, Electronics Cooling®—The **2024 Spring Edition** is distributed digitally at no charge to engineers and managers engaged in the application, selection, design, test, specification or procurement of electronic components, systems, materials, equipment, facilities or related fabrication services. Subscriptions are available through electronics-cooling.com.

LECTRIX®

EDITORIAL

Genevieve Martin
Associate Technical Editor of *Electronics Cooling Magazine*
R&D Manager, Thermal & Mechanics Competence, Signify

Navigating the Heat Wave in Technological Innovation for Electronics Cooling

Located in The Netherlands, we are constantly bombarded with press news concerning ASML, the giant chip machine developer. ASML is rolling out its new $350 million High NA (numerical aperture) EUV (extreme UV) machine, which is the size of a double decker bus. In order to keep Moore's law going, innovation must continue in the chip industry. This means that there will be no stop in the coming decades in the development of even more sophisticated electronic products.

Furthermore, sustainability and global warming are currently at the center of political discussions, and awareness of these issues is emerging within the industry. Electronics are more than ever at the center of all our products, and as engineers, we know that where there is electronics, there is heat.

In this editorial, I would like to shed light on industry trends at the heartbeat of progress in the landscape of electronics, the technological challenges at the cutting edge of cooling of electronics, and how embedding new technologies could be the solution to addressing these challenges.

A few industry trends currently impacting the electronics industry and electronics cooling are:

- **The Rise of Edge Computing:** The demand for faster processing and reduced latency intensifies. Edge computing emerges as a pivotal trend. Robust systems, capable of processing data closer to the source, are required, projecting into a new era of efficiency and real-time responsiveness.
- **Artificial Intelligence and Machine Learning:** Mechanical product designers, software tool developers, and electronics component developers are finding ways to reap the benefit of new techniques to drive intelligent systems, from smart home to autonomous vehicles. The field is at the intersection of opportunities and challenges, depending on a narrow balance between innovation and ethical considerations at times.
- **Sustainability:** With the growing emphasis on sustainability, electronics engineers, and the industry as a whole, are tasked with creating eco-friendly solutions. In the field of electronics cooling, we mainly see research in enhancing material properties, using process differently, driving energy efficiency, and driving usage of materials, recycling, and waste management.
- **Education and Skills Development:** The pace of technological evolution requires continuous commitment to learning to stay at the forefront of innovation. Collaboration becomes crucial in ensuring that engineers are equipped to tackle emerging challenges. Electronics cooling requires collaboration across disciplines more than ever.

I would like to name a few industry trends currently impacting the electronics industry and electronics cooling:

Key challenges (already in scope for at least a decade)

Following the industry trends, electronics cooling has to become even more innovative in thermal management techniques, address miniaturization and heat density, make use of the opportunities offered by advancements in manufacturing processes, or new development techniques. Advanced thermal management techniques are paramount to redefine the boundaries of traditional cooling methods along with green cooling solutions (e.g., recycling heat for other purposes).

- **Miniaturization and Heat Density:** The trend toward smaller and more powerful electronic components is not new but remains a concern regarding heat density. Attempts to innovate materials for heat dissipation and offerings from new manufacturing process are key to enhancing thermal conductivity. Novel materials or re-engineered materials play a pivotal role in dissipating heat effectively and improving the overall reliability of electronic devices.

- **AI-driven Cooling Systems:** Artificial intelligence is being leveraged to optimize cooling systems.
- **Integration of Cooling in Design:** The integration of cooling considerations into the initial design phase is crucial. Adopting a holistic approach will not only deliver performance but also integrated systems.

As the electronic world continues to innovate and push the boundaries of what is possible, engineers in the cooling domain play a pivotal role in ensuring the reliability and longevity of electronic devices. By exploring and implementing cutting-edge cooling technologies, the field of electronics cooling is not only keeping pace with technological advancements but is also contributing to a more sustainable and resilient future.

Overall, it is clear that the electronics industry and electronics cooling face significant challenges in the coming years, but with innovation, collaboration, and a focus on sustainability, these challenges can be overcome.

This issue features articles that address industry challenges by integrating new manufacturing approaches into “conventional” cooling technologies. I hope you enjoy reading them.

Genevieve Martin

SEMI-THERM®

40th Annual Semiconductor Thermal Measurement, Modeling and Management Symposium

March 25-29, 2024 | San Jose, CA, US

Register now at www.semi-therm.org

Keynote Speaker

TIM SHEDD

Engineering Technologist, Office of the CTIO at Dell, **Tim Shedd** will share his insights on the topic "Driving Sustainable Scaling of Compute to 2030"

Expand your expertise with the top-rated short courses!

"Thermal Challenges and Opportunities of Advanced Packages and Microelectronics Systems. Figure of Merit and Applications." Dr. Victor Chiriac (Global Cooling Technolog Group), Alex Ockfen (Meta)

"Direct to Chip Liquid Cooling: Single Phase Water and Two-Phase Refigerant Cooling with Pumped and Passive Systems" Professor Alfonso Ortega (Villanova University), Dr. Luca Amalfi (Seguente Inc.)

"Fundamentals and Applications of Machine Learning in Thermal Management and Heat Transfer Technologies" Professor Van P. Carey (UC Berkeley), Professor Alanna Cooney (San Francisco State Univerity)

"Semiconductor Packaging and Thermals: Upcoming Challenges" Dr. Kyle Arrington (Intel)

"Navigating Thermal and Reliability Challenges in Chip Components for Automotive High-Performance Compute Systems" Dr. Fen Chen (Independent Automotive Reliability/Validation Consultant)

"Transient Thermal Analysis Using Linear Superposition" Roger Stout (Professional Engineer, Retired)

"Passive Two-Phase Cooling: Pulsating Heat Pipes and Loop Thermosyphons" Professor Emeritus John Thome (JJ Cooling Innovation Sàrl)

SPONSORS

Platinum

celsia™ Making Hot Technology Cooler

Diabatix

SIEMENS

Short course

ARIECA

Media

electronics COOLING

View the complete program at www.semi-therm.org

TECHNICAL EDITORS SPOTLIGHT

Meet the 2024 Editorial Board

VICTOR CHIRIAC, PhD | **GLOBAL COOLING TECHNOLOGY GROUP**

Associate Technical Editor

A fellow of the American Society of Mechanical Engineers (ASME) since 2014, Dr. Victor Adrian Chiriac is a co-founder and a managing partner with the Global Cooling Technology Group since 2019. He previously held technology/engineering leadership roles with Motorola (1999-2010), Qualcomm (2010 – 2018) and Huawei R&D USA (2018 – 2019). Dr. Chiriac was elected Chair of the ASME K-16 Electronics Cooling Committee and was elected the Arizona and New Mexico IMAPS Chapter President. He is a leading member of the organizing committees of ASME/InterPack, ASME/ IMECE and IEEE/CPMT Itherm Conferences. He holds 21 U.S. issued patents, 2 US Trade Secrets and 1 Defensive Publication (with Motorola), and has published over 110 papers in scientific journals and at conferences.

► vchiriac@gctg-llc.com

GENEVIEVE MARTIN | **SIGNIFY**

Associate Technical Editor

Genevieve Martin (F) is the R&D manager for thermal & mechanics competence at Signify (former Philips Lighting), The Netherlands. She has worked in the field of cooling of electronics and thermal management for over twenty years in different application fields. From 2016 to 2019, she coordinated the European project Delphi4LED, which dealt with multi-domain compact modeling of LEDs and, since 2021, is coordinating the AI-TWILIGHT project. She served as general chair of the SEMI-THERM conference and is an active reviewer and technical committee member in key conferences including SEMI-THERM, Therminic, and Eurosime. She has over 20 journal and conference papers and 16 worldwide patents.

► gmartin.sig1@gmail.com

ALEX OCKFEN, P.E. | **META**

Associate Technical Editor

Alex Ockfen is a simulation engineer at Meta (formerly Facebook), providing technical leadership for thermal and structural design of consumer electronics products. He held previous positions at Raytheon where he obtained experience in thermal management and electronics cooling of a wide range of aerospace and defense applications. He has more than 10 journal and conference publications, is an inventor on multiple patents, is a professional mechanical engineer, and is currently serving as program chair of the SEMI-THERM conference.

► alex.ockfen@fb.com

ROSS WILCOXON | **COLLINS AEROSPACE**

Associate Technical Editor

Dr. Ross Wilcoxon is a Senior Technical Fellow in the Collins Aerospace Advanced Technology group. He conducts research and supports product development in the areas of component reliability, electronics packaging, and thermal management for communication, processing, displays, and radars. He has more than 40 journal and conference publications and is an inventor on more than 30 US Patents. Prior to joining Rockwell Collins (now Collins Aerospace) in 1998, he was an assistant professor at South Dakota State University.

► ross.wilcoxon@collins.com

COOLING EVENTS

News of Upcoming **2024 Thermal Management Events**

MAR
25-29

SEMI-THERM

DoubleTree by Hilton San Jose | San Jose, CA

SEMI-THERM is an international symposium dedicated to the thermal management and characterization of electronic components and systems. SEMI-THERM provides knowledge covering all thermal scales from integrated circuits to facilities, fosters discussions between thermal engineers, professionals, and industry experts, and encourages the exchange of information on academic and industrial advances in electronics cooling.

► **semi-therm.org**

APR
7-10

EuroSimE 2024

Four Points by Sheraton Catania Hotel & Conference Center | Sicily, Italy

Join EuroSimE in Catania, Sicily, Italy for the 25th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems. Bringing together engineers, researchers and scientists involved in Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems.

► **eurosime.org**

APR/MAY
30-1

Ceramics Expo & Thermal Management Expo

Suburban Collection Showplace | Novi, MI

Whether you're involved in producing, distributing, or maintaining thermal management solutions, Thermal Management Expo is designed for you. Harness the potential of cutting-edge materials and technologies to enhance your application capabilities, guaranteeing optimal performance and longevity. Forge new connections and partnerships with innovative suppliers and industry experts. Meet engineers, decision makers, end-user OEMs, and buyers from across the globe in person, facilitating valuable interactions. Easily find and compare products on our exhibition floor, streamlining your sourcing process. Your free registration will give you an all-access pass to not only Thermal Management Expo but also to Ceramics Expo, North America's leading event for the technical ceramic supply chain. Ceramics Expo brings together attendees and 250+ leading suppliers & manufacturers spanning every key end-user sector including aerospace, defense, automotive, energy and medical.

► **thermalmanagementexpo.com**

Effect of Thermocouple Size

Ross Wilcoxon
Associate Technical Editor for *Electronics Cooling*
Collins Aerospace

Thermocouples are widely used for temperature measurements. They are particularly useful in lab testing, due to their relatively low cost and the ability to easily fabricate thermocouples of specific lengths for a given test. This Tech Brief discusses issues related to the size of a thermocouple that may be considered when using them.

A thermocouple consists of two wires made of different metals. The wires are welded together at one end and, due to the Seebeck Effect, this junction of dissimilar metals generates a small voltage (typically of only a few millivolts). Since the voltage is a function of the junction temperature, the thermocouple produces a temperature response that can be measured relatively easily, which led to their being adopted for temperature measurements more than a century ago [1].

Originally, thermocouple circuits were typically comprised of three wires in series (such as copper – constantan – copper) that included two junctions of dissimilar metals. One junction would be attached to the location where the temperature was to be measured and the other junction held at a reference temperature (typically ice water). Each junction generated a voltage, but with opposite polarity so that the net voltage generated by the circuit corresponded to the temperature difference between the two junctions. The actual measurement does not directly determine the voltage generated by the thermocouple junctions but instead determines the voltage that must be applied to the circuit to produce zero current flow. The magnitude of this voltage is equal to that generated by the thermocouple junction, but with the opposite sign. Since the applied voltage results in no current flow, there is no electrically resistive loss in the thermocouple wires. Thus, the length of the thermocouple does not affect the measurement. In practice today, thermocouple meters include circuitry that provides this voltage balance, converts the voltage to a temperature measurement, and applies an internal reference temperature that eliminates the need for an ice bath[1].

Basic information on thermocouples is available from many resources, such as references [2, 3, 4]. These provide information on topics including the materials used in different thermocouple types, their measurement sensitivity, temperature limits, etc. However, these introductory overviews don't necessarily discuss details such as the impact of the size of thermocouple wires on measurements. For example, one of the cited references stated that "(thermocouples) do not conduct much heat away from a contact point" [2]. This is generally correct, but it depends on one's definition of 'much.' This Tech Brief gives quantified answers as to what 'much' may be for a thermocouple heat sinking effect.

When attached to a heat source, such as an electronic component, thermocouple wires can be described as thin metal structures that extend into the surrounding air. This is also an appropriate description of cooling fins, i.e., thermocouple wires can act as fins that dissipate power. They therefore somewhat cool the component being measured and reduce its temperature.

For example, *Figure 1* shows images of a circuit board in a thermal test. The top image shows an infrared (IR) image of the entire board while the bottom image shows a close-up of two components that dissipated the same power. Two sizes of Type-T thermocouples[2] were attached to the two components: the top thermocouple had 30 gauge wire (0.254mm / 10 mil diameter) while the bottom thermocouple had 40 gauge wire (0.0787mm / 3.1 mil diameter).

The top of *Figure 2* shows a close-up of the IR image of the two thermocouple components (the image has been rotated 90°C counterclockwise) and the bottom image in the figure shows a temperature scan along the horizontal slice depicted with the blue/red line. This image shows 'dips' on the two components; these dips are caused by the two thermocouples that locally cool the components by acting as fins. The larger (30 gauge) wires cause a much larger temperature dip of ~3°C while the smaller (40 gauge) wires only caused a temperature dip of ~0.9°C. The relative thermal

---

[1] 30+ years ago, the University of Minnesota Mechanical Engineering department had an ice machine to make ice for thermocouple reference temperature baths. Ice from this machine was also occasionally used for chilling beer during unofficial Friday afternoon graduate student 'colloquia'. Presumably, today's grad students no longer have this perk.

[2] Type-T thermocouples are made of a set of copper and constantan wires.

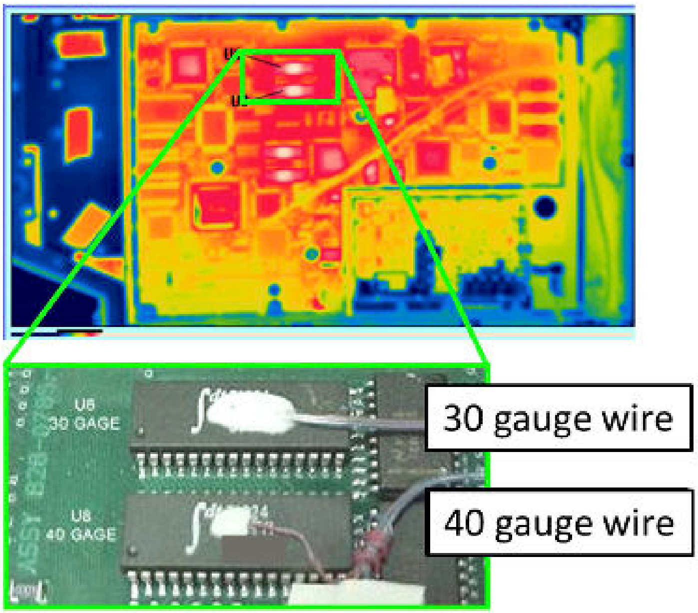


Figure 1: Thermocoupled components on a test board

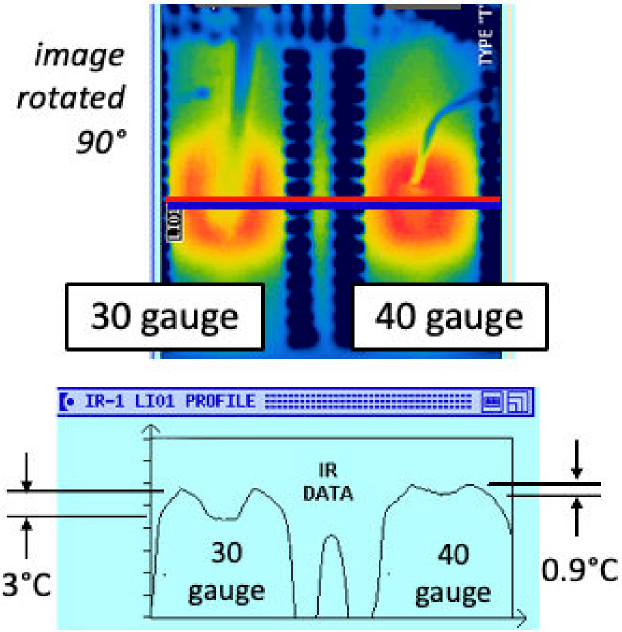


Figure 2: Temperature dips on thermocoupled components

loss in the thermocouples is also illustrated by the larger length of the 30 gauge wire that is yellow and green while the 40 gauge wire is primarily blue in the IR images of *Figure 2*. Note that the temperature profile shows two apparent temperature dips between the components; these are due to the low emissivity of the electrical leads on the components.

The test results shown in the previous figures indicates that thermocouple size can affect the temperature being measured. This is certainly not a new finding: other researchers have pointed out that larger thermocouples will cause a temperature drop [5] and that the effect also depends on thermocouple type [6].

To quantify the heat loss from a thermocouple, we can use fin equations to estimate the thermal loss from it. The thermal dissipation (Q) from an insulated tip fin is calculated as

$Q=M*\tanh(mL)$, where:

$M = (hPkA_c)^{1/2} * \Delta T$ and $m = (hP/kA_c)^{1/2}$.

In these equations, L is the length of the fin, h is the convection coefficient, P is the perimeter of the wire (πD), where D is the wire diameter, k is the wire thermal conductivity, and A_c is the wire cross sectional area ($\pi D^2/4$).

For a 30 gauge thermocouple (0.254mm diameter) that is 4" long (10cm) and in contact with a surface at 100°C while exposed to 25°C ambient air with free convection (assuming the convection coefficient is 10 W/m^2K), the heat transfer from a copper (k=390 W/mK) wire would be 28.7mW and 6.91mW from a constantan (k = 21 W/mK) wire. The actual thermocouple length has little impact on the results – the wire is essentially at ambient temperature within 1-2 cm. The total thermal loss from the two wires that make up a type-T, 30 gauge thermocouple is then ~35.6mW. In comparison, the smaller 40 gauge wire would only lose ~6.3mW to the ambient temperature. If the thermocouple wires are exposed to fan cooling that increases the convection coefficient to 40 W/m^2K, the thermal losses for the 30 and 40 gauge thermocouples are calculated to be 73.4 and 12.7mW, respectively.

Careful readers may point out that thermocouples generally are not bare wires, but are insulated. One would think that this electrical insulation thermally insulates them and reduces thermal loss. Somewhat surprisingly, analyses (both one-dimensional radial conduction and finite element modeling) indicate that the insulation around the bare wires actually increases the thermal loss by 30-50% compared to bare wires. This is a result of the larger surface area, due to the insulation, reducing the convective resistance more than conduction through the insulation adds resistance[3].

---

[3] This critical radius of insulation [7] effect is interesting enough that it could be a topic of a future Tech Brief.

Note - The images used in Figures 1 and 2 were produced by staff in the Rockwell Collins (now Collins Aerospace) Heat Transfer Lab: Dave Dlouhy (retired) and Doug Twedt.

In summary, attaching a thermocouple to a power-dissipating component will lead to some thermal loss into the thermocouple wires, which reduces the local temperatures. The size and type of thermocouple will impact the magnitude of the temperature drop. Type-T thermocouples, which have a copper wire, will have more thermal loss than other types. Using smaller thermocouples, such as 40 gauge instead of 30 gauge, will reduce the amount of thermocouple 'dip'. However, these smaller thermocouples are more delicate, so their non-junction ends are typically soldered to larger thermocouple wires for routing to the data acquisition system.

Figure 3 compares the expected thermal losses for different thermocouple types and sizes when used to measure a temperature 100°C above the surrounding air. These estimates were based on calculations for bare wires; as mentioned previously, insulation will likely increase the loss. The thermal loss due to thermocouples is generally a few tens of mW or less, so it can be ignored for parts that dissipate a few W. But if thermocouples are used on small parts that dissipate a few hundred mW, a large thermocouple can have a noticeable effect on the measured temperature.

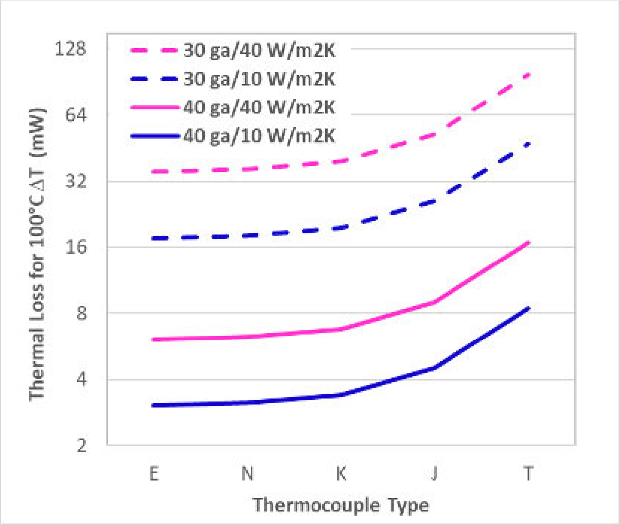


Figure 3: Estimated thermal loss for different thermocouples measuring a temperature 100°C above ambient

---

References

[1] L.B. Hunt, "The Early History of the Thermocouple", Platinum Metals Rev. 1964, 8, (1), 23; https://technology.matthey.com/article/8/1/23-28

[2] Steve Roberts, "Thermocouple Basics Part 1: Advantages to Multi-Channel Isolated Thermocouples", *Electronics Cooling Magazine* Blog, July 18, 2023; https://www.electronics-cooling.com/2023/07/advantages-to-multi-channel-isolated-thermocouples/

[3] Steve Roberts, "Thermocouples Basics Part 2: How They Are Made and Its Measurement System", *Electronics Cooling Magazine* Blog, July 26, 2023; https://www.electronics-cooling.com/2023/07/35284/

[4] "Thermocouple Probes", Omega Engineering, https://www.omega.com/en-us/resources/thermocouple-hub

[5] Q. He, S. Smith and G. Xiong, "Thermocouple attachment using epoxy in electronic system thermal measurements — A numerical experiment," 2011 27th Annual IEEE Semiconductor Thermal Measurement and Management Symposium, San Jose, CA, USA, 2011, pp. 280-291

[6] W. Tian, M. Berktold, C. Carte and E. Tan, "Investigation on Reading Discrepancy of Type T and Type J Thermocouples," 2020 19th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), Orlando, FL, USA, 2020, pp. 905-908

[7] Frank White, "Heat Transfer", Addison-Wesley, (1984), pp. 61-63

The Applicability of JESD51-14 for the Determination of Junction to Case Thermal Resistance

Robin Bornoff
Siemens Digital Industries Software

Rjc (or sometimes ThetaJC, θjc, Rth_jc), the so-called 'junction to case' thermal resistance, is a thermal metric that enables comparison of the thermal performance of packaged semiconductor devices from differing suppliers. The JEDEC standard JESD51-14 [1] documents a method for the experimental determination of Rjc. Although applicable for packages that exhibit a predominantly one-dimensional (1D) heat flow path (e.g. power packages), its repeatability makes it an attractive option to be applied more widely. So how valid is JESD51-14 for a wider range of package styles and what really is meant by a 1D heat flow path?

Steady State vs. Transient Rjc Measurements

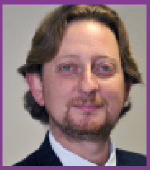
The classical definition of thermal resistance is the temperature difference between 2 iso-thermal surfaces divided by the heat that flows through those surfaces when in a steady state. For Rjc, one of those temperatures is the junction temperature, usually measured by applying JESD51-1, the electrical test method. The other temperature is the case temperature, the temperature at the center of the peripheral surface of the package through which the majority of heat passes. Depending on the package style, this might be the top face that has a heatsink attached or the bottom face that would be soldered to the PCB. Case temperature is usually measured using a thermocouple embedded at the interface of the case face and the object that it is attached to. It is worth noting that there is currently no published JEDEC standard that documents this method.

JESD51-14 is an alternative approach that is best described as a 'transient dual interface method' (TDIM). Here, only the junction temperature is recorded, but two transient measurements are made. The difference between the two measurements is due to a change in the interfacial resistance at the case face. This is usually realised by first applying some thermal interface material (e.g. paste) on the heatsinked case face, and then not. Rjc is denoted by the point at which the resulting Zth response curves deviate (effectively the point that the transient junction to ambient thermal resistances deviate).

Both methods are summarised in *Figure 1*. Here a package is considered on a low thermal conductivity board and heatsinked via a coldplate attached to its top case face. Note that, in lieu of physical measurements being used, this article instead employs a conjugate heat transfer thermal simulation-based approach.

How 'Accurate' is JESD51-14?

How does the value of Rjc determined by JESD51-14 compare to that from the steady state approach? Maybe it's wrong to ask how 'accurate' JESD51-14 is, as that would imply that the steady state value of Rjc is formally 'correct'. It could be argued that, due to the non-uniformity of temperature across the case face (regardless of the effectiveness of the heatsink), considering a single measured point temperature at the case face does not conform to the iso-thermal requirements of the definition of a thermal resistance. Despite this, one would at least expect the JESD51-14 Rjc value to be comparable to the steady state value.



Robin Bornoff

After receiving a bachelor's degree in Mechanical Engineering in 1992 and a PhD for CFD research in 1996 from Brunel University in the UK, Robin joined Flomerics as a Flotherm support and application engineer. By the time of the acquisition of Flomerics by Mentor Graphics in 2008 he was the Product Marketing Manager for Flotherm. Now in Siemens Digital Industries Software, he is an Innovation Roadmap Manager in the Simulation and Test Solutions division. With over 25 years experience in the field of electronics thermal simulation, he has published over 30 journal and conference papers and has had 7 patents granted.

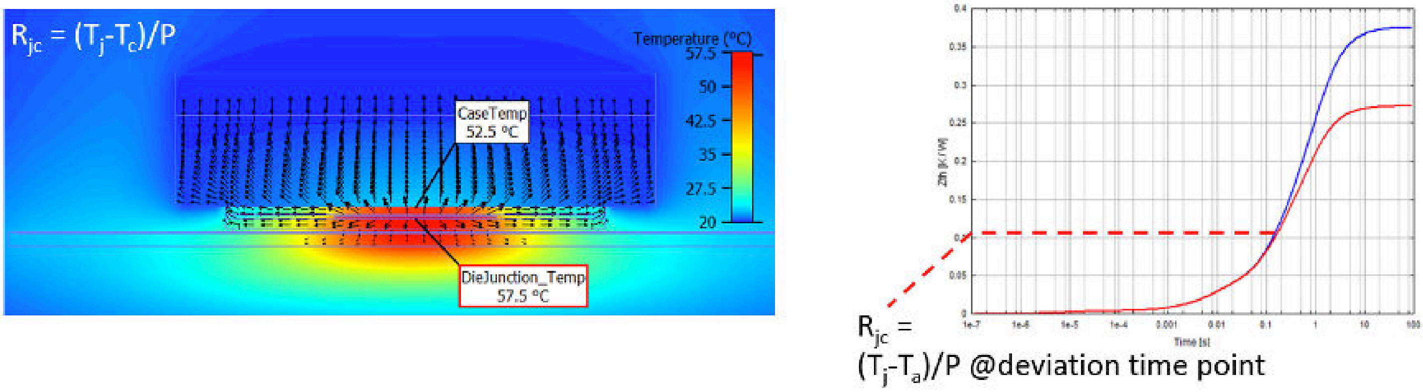


Figure 1: Steady state (top) and JESD51-14 (bottom) determination of Rjc

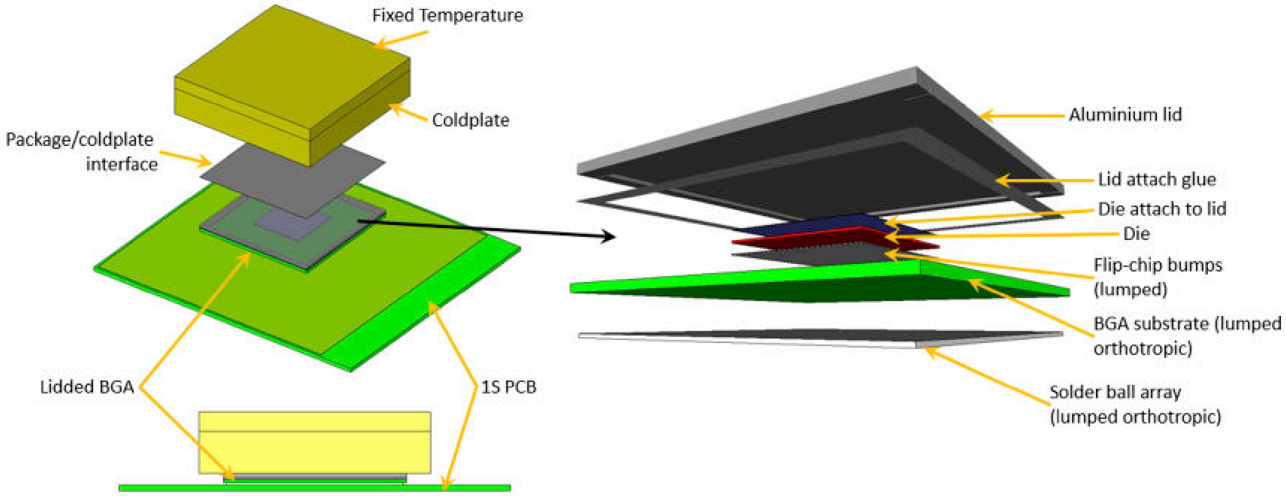


Figure 2: BGA Style Package (Lidded)

JESD51-14 Applied to a BGA Style Package

The applicability of JESD51-14 to power package styles, such as TO-263, D2PAK etc., is well documented [2]. How though would a BGA style package fare when its Rjc was determined using the TDIM as compared to the steady state method? Two typical BGAs were considered, one with a metal lid (*Figure 2*), the other identical but with an epoxy overmold instead of the lid. Both were attached to a low thermal conductivity (as per JESD51-3) board and heatsinked using a coldplate [3].

	Steady state Rjc (K/W)	JESD51-14 Rjc (K/W)
Lidded BGA	0.05	0.05
Overmolded BGA	1.79	0.82

Table 1

Table 1 summarises the simulated Rjc values as determined by the steady-state method and JESD51-14, for both BGA variants.

The lidded BGA JESD51-14 Rjc value corresponds exactly to that determined using the steady-state approach. However, for the overmolded BGA, the JESD51-14 Rjc value is about half that of the steady-state approach. If one considers the 1D heat flow requirements of JESD51-14 then, despite the relative complexity of the lidded BGA topology, it still must conform to this requirement. For the overmolded BGA, is it more erroneous due to the fact that Rjc is simply higher, or that it is less 1D in nature, due to the ratio of Rjc to Rjb (the thermal resistance from junction to board)?

Rjc vs. Rjb

Does a 1D heat flow just entail all the dissipated heat flowing from the junction through the heatsinked case face of a package? For that to occur, surely all that's required is that Rjc << Rjb?

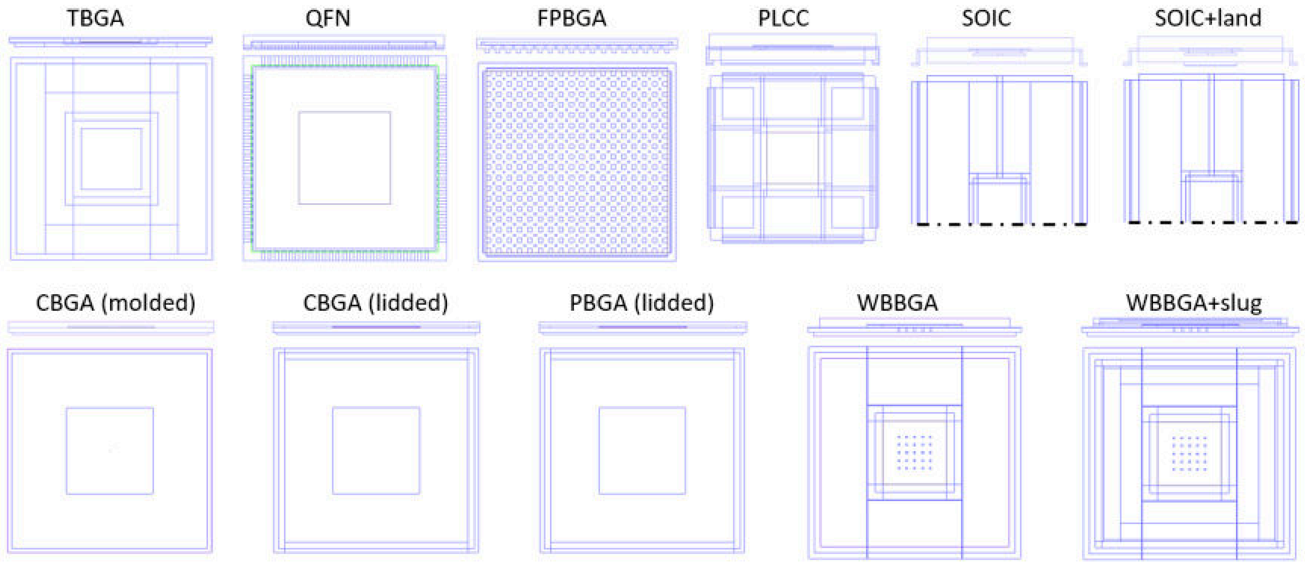


Figure 3: An Extended Range of Package Styles Considered

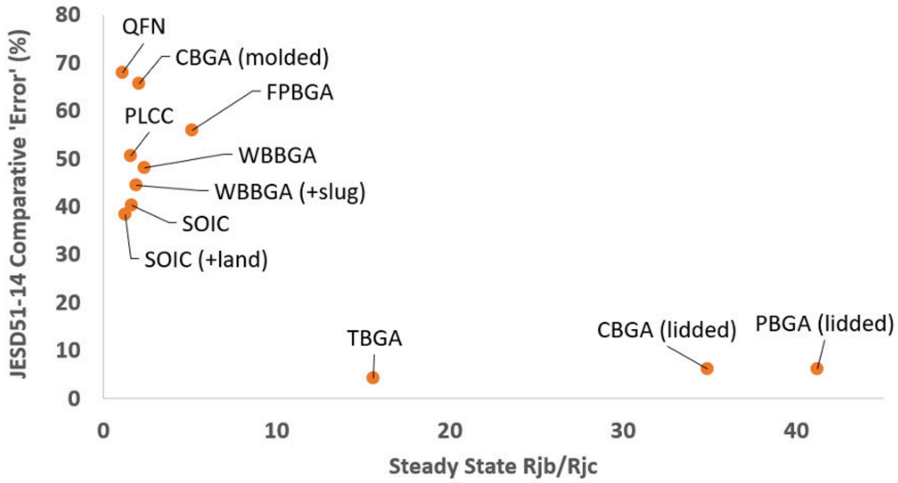


Figure 4: The Comparative 'Error' of a JESD51-14 Rjc Value vs. the Ratio of Rjb to Rjc

---

Is that therefore the criteria for determining the applicability of JESD51-14?

To answer these questions, an extended range of package styles were therefore considered (*Figure 3*).

JESD51-8 [4] documents the method to determine Rjb, utilising a ring cold plate to achieve a steady state heat flow down through the package and into a high thermal conductivity board, with the board temperature measured 1mm from the longest side of the package. This configuration was replicated in the simulation model and Rjb values were determined for each of the above package styles. Similarly, both JESD51-14 and steady-state Rjc values were determined by simulation. *Figure 4* plots the 'error' of the Rjc value determined with JESD51-14, as compared to the steady state value, against the ratio of Rjb to Rjc.

All JESD51-14 Rjc values were lower than the steady state Rjc values. For the three package styles that had a (steady state) Rjb/Rjc > 10, the error of a JESD51-14 Rjc value was < 6%. All others had errors > 40%. So, at least for the typical packages considered, JESD51-14 does appear to be applicable when Rjc is substantially lower than Rjb.

Metrics vs. Models

Whereas a metric should be used for comparative purposes only, there is still the obligation that it reflects, to some extent, the thermal performance of a package. It might be (mis)used for predictive purposes, but then any modelled temperature would only be valid for exactly the same thermal environment that was imposed for the extraction of that metric.

When using simulation to predict operational thermal performance, a thermal model should be used instead. From simplistic 2-resistor models [5], Cauer RC ladder type models [1] through to boundary condition independent DELPHI type models [6] and state-of-the-art ROM models [7] there are many options to choose from. All of which however are either predicated on the availability of models from a component supplier or require the end-user to extract the models themselves from a combination of measurement and simulation.

Conclusion

Not suffering the complications and lack of reproducibility of case temperature thermocouple measurements, JESD51-14 is an attractive approach for Rjc determination. Its general applicability may well reach beyond just common power packages, so long as the heat flow is predominantly 1D, which in turn might be characterised by Rjb/Rjc > ~10.

References

[1] https://www.jedec.org/standards-documents/docs/jesd51-14-0

[2] https://www.electronics-cooling.com/2010/09/transient-dual-interface-measurement-of-the-rth-jc-of-power-semiconductor-packages/

[3] R. Bornoff, "Application of JESD51-14 to BGA Package Styles," 2022 38th Semiconductor Thermal Measurement, Modeling & Management Symposium (SEMI-THERM), San Jose, CA, USA, 2022, pp. 48-54.

[4] https://www.jedec.org/standards-documents/docs/jesd-51-8

[5] https://www.jedec.org/standards-documents/docs/jesd-15-3

[6] https://www.jedec.org/standards-documents/docs/jesd-15-4

[7] L Codecasa, V d’Alessandro, A Magnani, N Rinaldi, PJ Zampardi, “Fast novel thermal analysis simulation tool for integrated circuits (FANTASTIC)”, 20th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC) article 6972507 United Kingdom, 2014.

Adding Function, Value, and Performance to Direct-to-Chip (DTC) Cold Plates With Ultrasonic Additive Manufacturing

Lance Dumigan
Fabrisonic, LLC

Mark Norfolk
Fabrisonic, LLC

Practical Knowledge Gained

"The performance of DTC cold plates can be enhanced by a new method of fabrication called Ultrasonic Additive Manufacturing (UAM). Building DTC cold plates with UAM could enhance performance and functionality."

The direction of Artificial intelligence and High Power Computing (AI/HPC) is driving greater computation and power requirements, resulting in greater heat generation. With the emergence of Large Language Models (LLM), computational power is more important than ever. A.I. that generates text, images, and media requires larger computational power, memory, and higher infrastructure costs. [1] The current trend for AI/HPC servers, with a power usage of 20-40kW [2] per rack, challenges conventional air cooling technologies. AI/HPC data centers have been moving toward Liquid Immersion (LI) and Direct-To-Chip (DTC). LI is the emersion of a rack, or cluster, into a liquid, and DTC is attaching a water-cooled cold plate that extracts heat directly from the electronic device (GPU/CPU). Of those two options, DTC would lend itself to a new build and a retrofit to existing servers.

As these servers see higher power and density increases, they must be met with an increase in cooling capacity. Data center operators must install the infrastructure to accommodate this new dynamic. These higher densities are projected to be as high as 50–100 kW

Lance Dumigan
Lance is an Electrical Engineering graduate of Rochester Institute of Technology. After graduation, he entered the Naval Aviation program as a naval aviator and Patrol Plane Commander of 12 aircrew members, operating the P-3 Orion from military and civilian bases around the Pacific Ocean and Indian Ocean basin. Following his active duty tour, Lance entered the private sector, where he held positions of Product Manager, Sales Engineer, Product Engineer, Sales and Marketing Manager, Product Marketing, and Business Development Engineer with several start-up companies and start-up ventures in his background. Lance has worked in telecommunications, power conversion, automation, machining, and additive manufacturing markets.

Mark Norfolk
Mark brings over 25 years of diversified experience in R&D, manufacturing, and shop floor management. Currently serving as President and CEO at Fabrisonic LLC, he spearheaded the commercialization of Ultrasonic Additive Manufacturing (UAM) Technology. Before Fabrisonic, Mark held a pivotal role as a Senior Project Manager at EWI, managing projects for the U.S. Navy Joining Center and overseeing diverse R&D programs for governmental and commercial clients, including the U.S. Department of Energy and the Ohio Department of Development. His career commenced at John Deere, where he innovated vehicle structural testing methods and later led corporate-wide virtual manufacturing. Mr. Norfolk holds a B.S. in Welding Engineering from The Ohio State University and an MBA from the University of Iowa. He is a licensed Engineer and certified Project Management Professional.

per rack. DTC cold plates must meet these higher heat extraction requirements. There is greater pressure on DTC cooling to extract heat from CPUs, GPUs, and memory. According to Gartner Research, Rack power densities could reach as high as 100kW as A.I. models and synthetic data need greater processing capacity. [3] Looking further into the future, primary and secondary loop water pressure, flow, and even capacity will be considerations that will need to be addressed. While increasing the diameter of the manifold 2x would enhance the flow distribution by as much as 10% [4], those looking into the future of data centers see water conservation as a growing priority [5]. With the cost of modern processors approaching $15k per device (or higher), optimizing their performance is essential when multiplying the number of processors per server and the number of servers per rack.

Considerable research and discovery have been performed concerning the DTC option. The cooling plate flow distribution, flow rate, thermal hot spots, temperature uniformity, microchannel plates, and different flow schemes have been evaluated [6]. Companies such as JetCoolTM, AsetekTM, SupermicroTM, and many others have products for a DTC solution. However, a highly relevant and little-known additive manufacturing (AM) process is poised to enhance the effectiveness of the existing DTC technologies. The AM process that offers this enhancement is referred to as Ultrasonic Additive Manufacturing (UAM) [7]. UAM offers several capabilities that could be employed to accelerate the extraction of (energy) heat in a DTC cold plate. As UAM can combine dissimilar metals, embed sensors and materials, and print cold plates from a few inches to a few meters with complex internal geometries with smooth (machined) passages, this technology's application represents the potential for significantly increased DTC cold plate performance.

Most people are familiar with Additive Manufacturing (AM). The most widely known forms of AM use a metallic powder that is solidified through the addition of heat energy (laser, for example), which melts the powder in-plane and builds the shape by melting one layer of powder upon the other. Other methods include using an adhesive or binder to create a shape for each layer and then building successive layers to create the shape (product). UAM uses metal foils in a sheet-fed process where a shape or product is built with layers of metal foil without adding heat or melting the metal. Because the UAM process is unlike fusion-based AM processes, the UAM process does not melt the metal, so there is no change to the metal microstructure. This process allows the layering of multiple metals in one component. This aspect of UAM is highly advantageous for DTC cold plates.

The three components of one UAM weld head system are the "horn," the transducers, and a set of brackets [*Figure 1*]. The horn is a highly engineered piece of tool steel designed to resonate at 20KHz. The transducers oscillate the horn with up to 9kW of power, and the brackets apply a downward force of up to 10K Newtons. During the build process, the horn is rolled over thin sheets of metal foil. As the horn is rolling over the sheet of metal (along the X-axis), the transducers oscillate the horn (on the Y-axis) while the brackets are applying a downward pressure (negative Z-axis). The oscillation "scrubs" the two metal layers together, dispersing the oxides and impurities. This action keeps the metals in a solid state while increasing their plasticity. The downforce allows the two metals, while plasticized, to bond together metallurgically. The most important result of this process is that the bond between the two metals (whether they are similar or dissimilar metals) is a full metallurgical bond with no intermetallic formation [8]. These pure metallic bonds mean there is no resistance to the transfer of electrical or thermal energy as expected from using a braze or solder. The net effect of this process is the true differentiator. A part will be one monolithic piece of metal formed from similar or dissimilar metals. Additional sustainability benefits to the UAM process will not be explored here. UAM provides thermal engineers with three distinct advantages:

- Freedom of Geometry
- Freedom of material
- Freedom of information

Freedom of Geometry

While UAM weld heads have been integrated into a variety of motion systems, a typical UAM system is installed into a CNC Mill. This configuration, called "Hybrid Manufacturing," could be the breakthrough technology to increase DTC heat extraction. Combining UAM, an additive process, with a CNC mill, a subtractive process, allows for manufacturing complex interior channels, fins, turbulators, and evaporation geometry where every surface has a CNC surface finish and CNC accuracy [*Figure 2*]. Fusion-based 3D printers also allow freedom of geometry, but parts manufactured with that type of (AM) process have high surface roughness and wide dimensional variation. UAM allows designers the freedom to create the exact geometry they need at the exact location they require, with a CNC-quality finish.

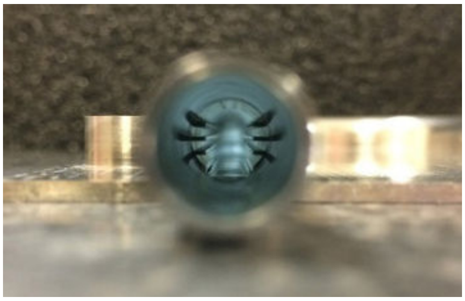


Figure 1

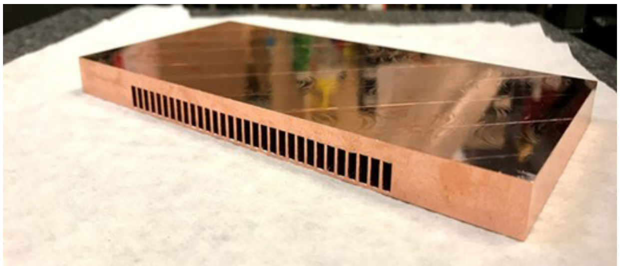


Figure 2

Freedom of Material

UAM allows designers to put the metal they need where they need it. UAM does not rely on melting, so it avoids the complex metallurgical interactions of most welding processes. As a result, every layer in a UAM build-up (part) can be made from a different metal [*Figure 3*]. Many UAM heat exchangers are made with aluminum to reduce cost, and copper is printed in specific locations to wick heat away from a specific heat source. Similarly, materials with low coefficients of thermal expansion, such as Invar and Molybdenum, have been layered into heat exchangers to help mitigate CTE stresses between chips and metal cooling structures [*Figure 4*].

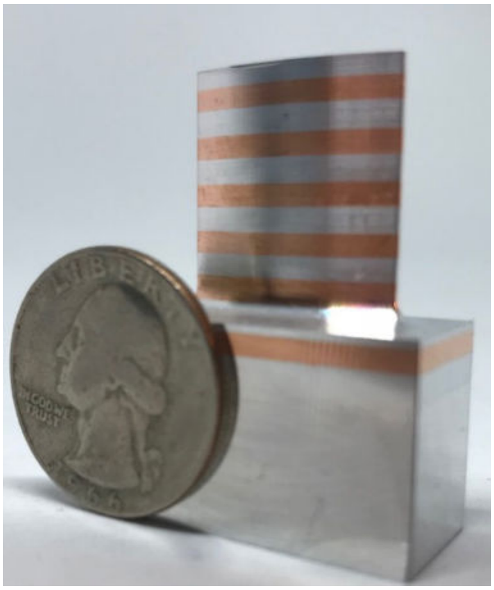


Figure 3

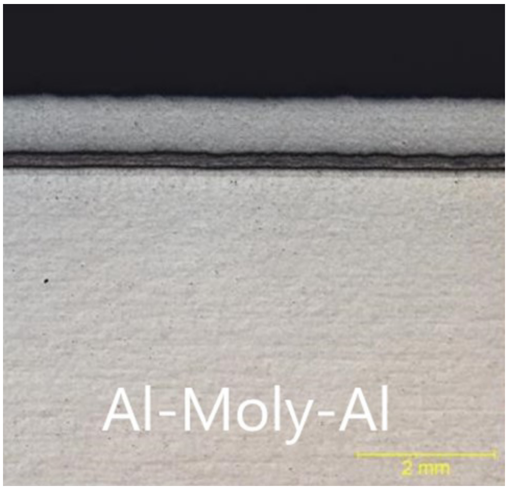


Figure 4

While copper has proven to be an excellent conductor (~400 W/m K) to extract heat from high-power electronics, many new higher-conductivity materials are emerging. UAM has the unique ability to embed one material inside another. That merges the properties of both materials to create a hybrid material designed by the engineer and made by the UAM system. Relevant to the construction of a DTC cold plate, various carbon-based materials could be embedded within the architecture of an aluminum or copper DTC cold plate. This material freedom could significantly enhance heat transmission from the device into the cooling liquid. Recent experiments with superconducting foils embedded into copper using a UAM process have shown great promise for creating high-performance laminates for electrical and thermal conductivity [9]. Simple combinations of aluminum, copper, and silver can be combined with UAM to extend the range of existing components. New materials such as graphene and superconductors embedded in DTC Cold plates could provide orders of magnitude higher heat flux.

Freedom of Data

The low-temperature nature of the UAM bond allows the embedding of sensitive electronics anywhere in a solid metal part. By embedding sensors directly into a heat exchanger, operators can get real-time in situ data for structural health monitoring, condition-based maintenance, or performance monitoring. In other industries, UAM has been used to embed fiber optic cables for sensing strain and heat. The sensors allowed the customer to measure strain and temperature throughout a complex engineering process. Other applications include embedding sensors in the wall of process piping for oil/gas and nuclear industries. Similar fiber optic sensor arrays would allow early detection of an overheated electronic device (GPU, CPU) within a DTC cold plate. Incorporating real-time data could play an integral role in a "smart" water flow manifold system that could direct the coldest inlet water to the server (or device) in real-time.

The design freedom that UAM provides has already been leveraged in high-consequence environments such as satellites. NASA significantly improved the performance of a satellite heat exchanger [10] [*Figure 5*] by over 30% with a simple UAM redesign. Similarly, UAM was employed to create a heat exchanger for Cube Satellites [11] for Utah State University with a combination of aluminum and copper. Similar concepts could be extended directly to DTC cold plates using other materials [*Figure 6*].

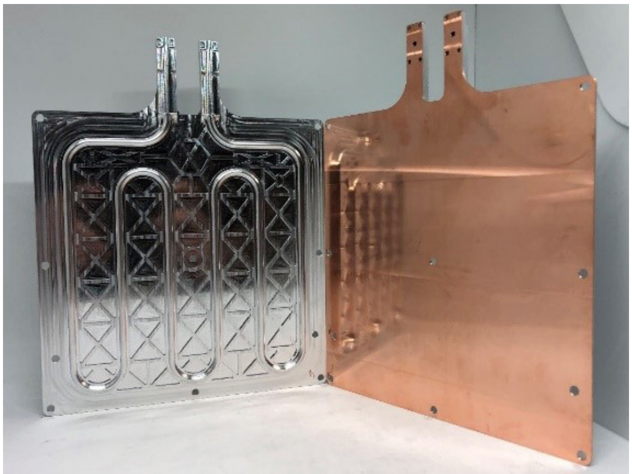


Figure 5

UAM can embed materials, devices, and sensors that have yet to be investigated in DTC cold plates. Accelerating heat extraction along with temperature sensing at critical points on and around the CPU/GPU, the server, and the rack, coupled with a software application that can leverage these sensors and embedded devices, could be the pathway to the next generation of DTC systems. As chip density increases, server densities increase, and rack power and heat increase, air cooling may fall short of the cooling required with these AI/HPC data centers. DTC offers a robust option. The current architecture of the DTC cold plates has been greatly optimized. More innovative approaches should be investigated, emphasizing maximizing chip cooling by further developing current DTC cold plates. Given the applications mentioned above and the technology already employed that directly relates to a DTC form factor, it would hold that UAM could help.

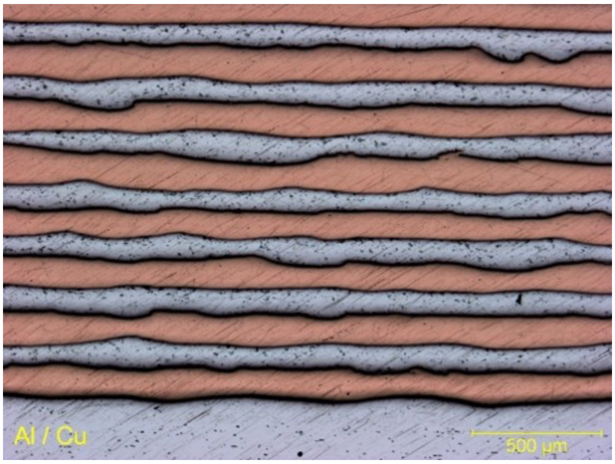


Figure 6

References

[1] Neptune.AI "Deploying Large NLP Models: Infrastructure Cost Optimization, "Nilesh Barla, March 2023, https://neptune.ai/blog/npl-modes-infrastructure-cost-optimization

[2] Data Center Frontier, Endeavored Business Media, LLC "Rack Density Keeps Rising at Enterprise Data Centers," Rich Miller, April 2020, https://www.datacenterfrontier.com/cooling/article/11429037/rack-density-keeps-rising-at-enterprise-data-centers

[3] Research North America, H1 2023, North America Data Center Report, Jones Lang LaSalle I.P., Inc

[4] Holistic Study of Thermal Management in Direct Liquid Cooled Data Centres: from the Chip to the Environment, Mustafa Alaa Kadhim Kadhim, The University of Leeds, Institute of Thermo-Fluids, School of Mechanical Engineering, Apr 2018

[5] Data Center Knowledge, "Is Chip Cooling the Answer to Data Center Sustainability?" Soni Brown, Aug 2023

[6] Thermal Science, "Design and analysis of liquid cooling plates for different flow channel configurations," Muhammad Farhan, Muhammad Amjad, Zia ulRehman Tahir, Zahid Anwar, Oct 2021

[7] https://gen3d.com/news-and-articles/the-seven-categories-of-am-processes/

[8] Comprehensive Review of Ultrasonic Additive Manufacturing, Adam Hehr, Ph.D, Mark Norfolk, Oct 2019

[9] 1 U.K. Atomic Energy Authority, Abingdon OX14 3DB, United Kingdom, 2 Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow G1 1XW, United Kingdom, Development Of UAM For Rebco CC Terminations In High Purity Copper, Y. Dieudonne1†, A. Shchukin2, M. Burkhart3, M. Norfolk3, Fabrisonic LLC, Lewis Center, OH 43035, USA, † Corresponding author: yannik.dieudonne@ukaea.uk

[10] Maghsoudi, Elham, Mastropietro, A. J., Roberts, Scott, and Kinter, Bradley, "Experimental Thermal Performance Comparison of 3D Printed Aluminum Heat Exchangers vs Traditionally Manufactured Heat Exchangers," Spacecraft Thermal Control Workshop (STCW), El Segundo, CA, March 2017

[11] Anderson, Lucas, Swenson, Charles, Mastropietro, A. J., Maghsoudi, Elham, Luong, Simon, Hofmann, Douglas, and Roberts, Scott, "Active CryoCubeSat Project: Design and Status," Small Satellite Conference, Logan, UT, August 2017

Blue Laser Welding Increases Vapor Chamber Fabrication Efficiency

Matthew Philpott, PhD
NUBURU, Inc.

We all understand that higher circuit density and increasingly compact microelectronic devices have created a need for more efficient cooling. Vapor chambers have emerged as a widely employed solution in some of the most demanding microelectronics applications. They are already found in high-performance computers, such as servers, workstations, and personal gaming desktops and laptops, as well as in mobile devices, including smartphones and tablets.

Vapor chambers are a form of planar heat pipe and operate in a manner like that of traditional heat pipes. Specifically, the operating circuitry heats a liquid within the heat pipe converting it into its gas phase. The heated gas physically moves away from the region where heat is produced through channels, carrying the heat with it. It then reaches a condenser located away from the active circuitry where the latent heat of the vapor is transferred out of the device, and the gas recondenses. The fluid circulates back to its original location to begin the process again.

Vapor chambers owe their success primarily to two key advantages as compared to other cooling methods, including traditional heat pipes. First, their thin, flat shape occupies less volume than a heat pipe. This makes them well-suited for use in highly space-constrained systems. Second, vapor chambers generally offer greater thermal transfer efficiency for a given area as compared to heat pipes. Furthermore, they typically can handle higher power densities (>50 W/cm²) are better and particularly useful for cooling circuitry with “hot spots.” Vapor chambers offer numerous other advantages, as well. For example, the thin shape of the vapor chamber makes them relatively insensitive to orientation, which is particularly useful for handheld and other mobile devices.

But, as the microelectronics miniaturization trend continues, there is a demand to make vapor chambers even thinner than current designs. This creates some challenges in terms of fabrication. One of these involves the welding process used in assembly of the most common vapor chamber configuration. This article explores how welding methods based on newly developed blue laser sources may provide a solution to this issue.

Vapor Chamber Production

Most vapor chambers in use today are formed from two separate, thin pieces of high thermal-conductivity metals. These are stamped to create the desired pattern of channels for fluid and gas flow. During assembly, these pieces are matched together, and the periphery of the assembly is sealed to complete the device.

For the device to function properly, it is essential that the two separate plates are joined with a hermetic seal. Additionally, the seam must be of sufficient mechanical strength to ensure that the integrity of the device is maintained over the lifetime of the product. In many cases, this means the seal must remain unbroken even in the presence of mechanical shock and vibration in addition to withstanding substantial temperature changes.

Currently, the most widely used production technique for joining the two plates is solid-state diffusion bonding. This process involves pressing the two plates together in a vacuum under high mechanical pressure and at an elevated temperature (but below the melting point of any of the materials involved). The

Matthew Philpott, PhD

Dr. Philpott has over 22 years of experience working in the commercial laser industry, and has held a wide range of roles in Sales, Marketing, Applications Engineering and Business Development. Dr. Philpott's cross-market expertise covers automotive/EV (electric vehicle) manufacturing, microelectronics manufacturing, and display manufacturing. Dr. Philpott holds a BS in Chemistry from Furman University and a PhD from the University of Washington in Physical Chemistry.

seam area on both plates must be prepared so that they are smooth and debris free.

Under these conditions, solid-state diffusion will cause atoms from the two surfaces to intersperse with each other creating a permanent bond. While diffusion bonding doesn't form a full fusion weld, the mechanical characteristics of the joint are still adequate for typical vapor chamber applications.

While diffusion bonding has long been used extensively and successfully, it does pose some drawbacks. One is the relatively long cycle time for evacuating the oven and heating the parts. It is possible to process several parts simultaneously, but as oven capacity increases, so does its capital cost and the amount of production floorspace it occupies.

Looking forward, the biggest issue with diffusion bonding is that thermal cycling tends to impart a permanent warpage in very thin copper vapor chambers. And, copper, with its high thermal conductivity, is by far the predominant material used for vapor chamber construction. This substantially limits the ability to continue using diffusion bonding as vapor chamber thicknesses shrink.

Laser Welding

Laser welding offers a possible alternative. This technique is already being successfully employed in several high-precision joining applications including numerous tasks, particularly in e-mobility and battery manufacturing, that involve joining thin metals.

For vapor chambers in particular, laser welding can deliver a substantially reduced cycle time. This is true even though it welds a single part at a time, rather than processing multiple parts at once, because the processing time per part happens within seconds.

While laser welding also requires fixturing for holding and clamping parts, these are generally much simpler than the tooling associated with diffusion bonding. This is because laser welding doesn't have the same requirement for exerting high pressure evenly over the entire weld path. The computer programmable weld path of a laser also makes it easier to create new tooling for new designs. Plus, it allows the flexibility of switching geometries on the fly in production to accommodate changing the clamp.

Laser welding produces a true fusion weld while diffusion bonding does not. Thus, the seal integrity and strength are generally better, although diffusion bonding generally delivers adequate results for this application.

Finally, laser welding is generally a "greener" method than diffusion bonding. Specifically, much less energy is required to run the laser system than needed for the large oven and pumps utilized in diffusion bonding.

Blue Laser Welding

Given the apparent advantages of laser welding, why hasn't it been widely adopted for vapor chamber production in the past? The problem again is associated with copper.

Copper is very highly reflective at the infrared wavelengths produced by the fiber or solid-state industrial lasers commonly used for metal welding. This is shown in the absorption graph in *Figure 1*.

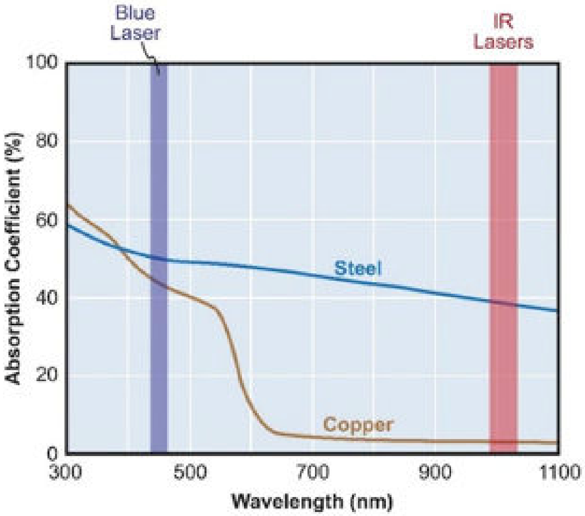


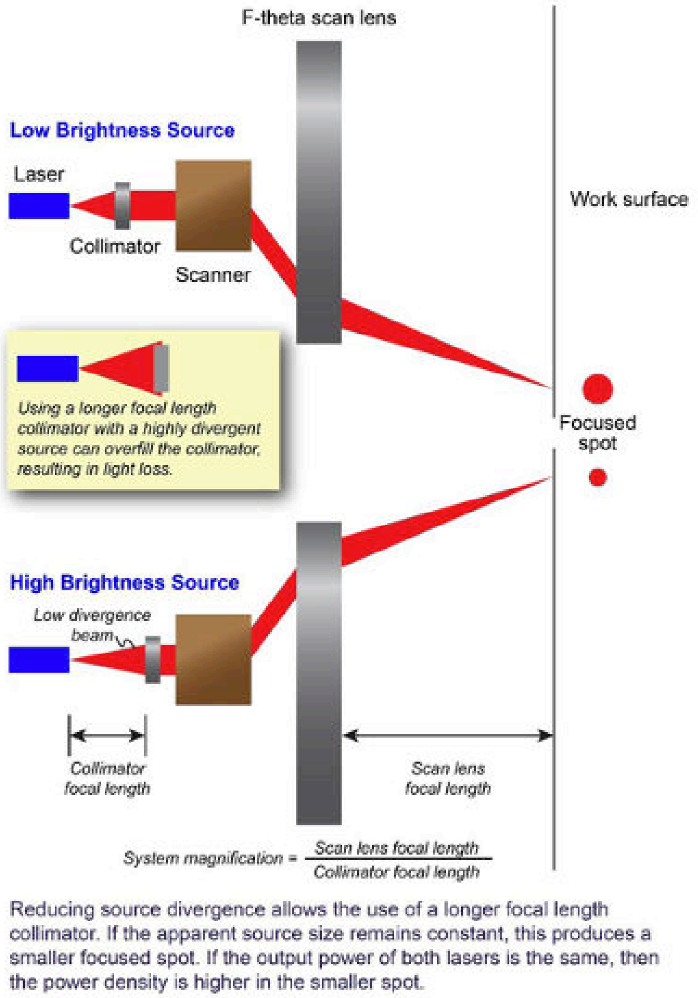
Figure 1: Visible and near infrared absorption spectra of copper and steel

This makes welding copper with infrared industrial lasers an inefficient process. A significant amount of power must first be delivered to the work surface melt it. This melted material absorbs infrared more strongly than the solid form. Continued absorption of laser light then vaporizes the copper. This initiates a process called "keyhole" welding, that's name is derived from the narrow aspect ratio that is seen in the shape of the interaction zone (the melt pool and associated vapor).

The large amount of energy that must be supplied to maintain the keyhole welding process makes it inherently chaotic and unstable. Bubbles within the melt pool can eject molten material, causing spatter on the material surface leaving voids or porosity within the weld seam itself. The process window is relatively narrow, and the total heat load introduced into the part is relatively high. This can cause permanent warping, making the method completely unusable with thin metals.

The graph also shows that both copper and steel (the second most popular material for vapor chamber construction) exhibit higher absorption at blue wavelengths. The absorption of copper, in particular, is 13X higher at 450 nm than at 1 µm. This means much less laser energy is required to initially melt the material and then keep it molten.

The result is that blue lasers can weld copper and steel in both the keyhole and more versatile "conduction" modes. The latter in-



Reducing source divergence allows the use of a longer focal length collimator. If the apparent source size remains constant, this produces a smaller focused spot. If the output power of both lasers is the same, then the power density is higher in the smaller spot.

Figure 2: A high brightness source can be focused to a smaller spot with higher power density

Figure 3: Top surface (top) and bottom surface (bottom) of a full penetration weld joining two 100 µm thick phosphor bronze plate. No spatter is seen

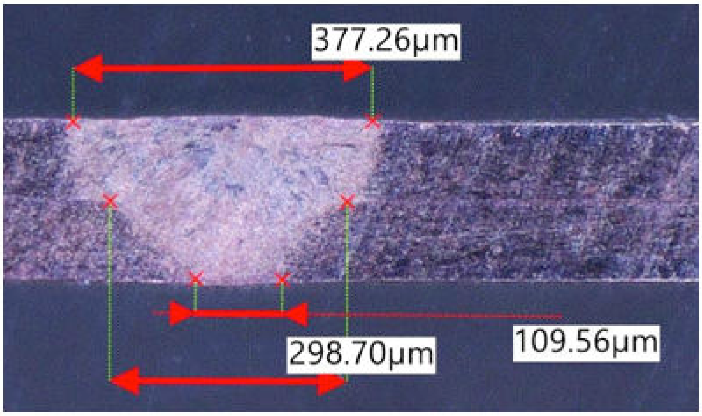


Figure 4: Cross section of a full penetration weld joining two 100 µm thick phosphor bronze plates. The weld is free of porosity and voids

volves melting the material, but not vaporizing it. This reduces the overall heat input so that part warping is avoided. Plus, the lower energy input makes the process more stable, consistent, and easy to control. The welds produced are free of spatter and voids.

Blue Laser Implementation and Future Trends

Blue lasers in the 500 W output power range have been successfully used for vapor chamber welding. These are focused on to the workpiece, and either the laser or part is moved so that the beam traces along the desired weld path.

The weld quality achieved with this approach is good and consistent, and the overall production throughput possible is competitive with diffusion bonding.

However, as vapor chambers get thinner, even blue lasers have faced limitations. Now, a new generation of higher brightness blue lasers has become available that can overcome this problem.

But what is high brightness, and why is it needed to weld thinner parts? High brightness is essentially a combination of high laser output power, small apparent source size, and low beam divergence. A high brightness laser can be focused to very small spot sizes to achieve high power densities, which is essential for many materials processing tasks. Furthermore, this tight focus can generally be achieved more easily (with simpler and less costly optical systems) and over longer focusing distances.

A key benefit of high brightness is that it provides more flexibility in terms of exactly how laser power (and therefore heat input) is delivered and spatially distributed at the work surface. This provides the finesse required to weld very thin materials without warping. In particular, a high brightness blue laser is uniquely able to weld very thin copper because its high absorption minimizes heat input, and its high brightness enables that small amount of heat input to be carefully managed.

Another important advantage of higher brightness is laser scanner compatibility. A scanner moves the weightless laser beam using galvanometer mirrors rather than by bulk motion of the workpiece or optics. This can deliver a dramatic increase in processing speed. It also facilitates the processing of larger sized vapor chambers, enabling complex weld seam shapes and the ability to switch product geometries on the fly.

Getting Higher Brightness

Creating this new class of higher brightness blue lasers has required a different approach than the ones used in the past.

Virtually all commercial blue lasers operate by combining the output from numerous Gallium nitride (GaN) semiconductor laser diodes that output at about 450 nm (blue). First generation blue lasers used either multi-emitter laser bars or commercially available modules containing multiple single emitters. In either case, the individual emitters are in fixed positions spaced relatively far apart. The inability to reduce the spacing between these emitters, and most importantly, to control the pointing and divergence of each individual source, limits the achievable brightness of these designs.

To overcome this limitation, manufacturers are now building blue lasers using large numbers of chip-on-submount laser diodes. Each chip-on-submount laser diode can be individually placed with high positional precision into an array with relatively small spacings between the sources. Furthermore, separate collimating optics can be placed over every single diode source. Each of these are independently adjusted to precisely control the divergence and pointing of every laser diode. This arrangement delivers a much higher brightness combined source.

Blue lasers based on individual chip-on-submount devices have now been successfully scaled up to the 1 kW level. They have sufficient brightness to weld very thin copper parts using scanning systems, which delivers the speed and flexibility benefits mentioned previously. This makes blue lasers a practical alternative to diffusion bonding for high volume welding of vapor chambers now and in the future as product dimensions decrease.

Summary of the IEEE ITherm 2023 Conference

John F. Maddox, Ph.D., P.E.
Associate Professor of Mechanical Engineering at the University of Kentucky, Paducah Campus

---

The IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm) was held at the JW Marriott Grande Lakes, Orlando, FL, May 30 – June 2, 2023. This was the 22nd ITherm, which was first held in 1988. The conference was historically held every other year until 2016 when it switched to an annual schedule. ITherm 2023 was sponsored by the IEEE Electronics Packaging Society (EPS). ITherm has partnered with IEEE EPS peer conferences, including the International Workshop on Thermal Investigations of ICs and Systems (THERMINIC) in Europe, and the Electronics Packaging Technology Conference (EPTC 2023) in Asia.

The ITherm 2023 program consisted of 16 professional development workshops and three full days of technical presentations in four tracks with 43 sessions in which 145 papers were presented. Additional technical events included three keynote addresses, five panels, five technology talks, a student poster competition, and a student heat sink design competition.

Keynotes

On the first day of the conference, Sandeep Ahuja, Sr. Principal Engineer in the Datacenter and AI Group of Intel, gave a keynote address entitled "Transformation of Data Centers from Air to Liquid Cooling" discussing the benefits and challenges of adapting data centers to liquid cooling to addressing modern compute loads.

On the second day of the conference, Griselda Bonilla, Senior Technical Staff Member (STSM) and Senior Manager of the Advanced Interconnect Technology group at IBM Research, gave a keynote address entitled "Innovative Chiplet Integration Technologies for HPC and AI Hardware Systems" describing the opportunities provided by chiplet integration to allow modular performance scaling.

On the final day of the conference, Steve Rickman, F NASA Technical Fellow for Thermal Control & Protection, gave a keynote address entitled "Space Mission Thermal Control and Protection Challenges – Past, Present, and Future" discussing thermal management in extreme environments ranging from near absolute zero up to 140,000 K.

Best and Outstanding Papers

Awards given for the best and outstanding papers in each track, based on judging from reviews and inputs from session and track chairs, were unveiled to the attendees.

Professor Avram Bar-Cohen Best Papers

Component Level Thermal Management

- Min Jong Kil (UCLA), Eythan Lam (UC – Santa Barbara), Mostafa Abuseada (UCLA), James F. Buckwalter (UC – Santa Barbara), Timothy S. Fisher (UCLA) "Direct Solar-Thermal Formation of Graphitic Heat Spreaders on Organic Substrates."

John F. Maddox, Ph.D., P.E.
Dr. John F. Maddox is an Associate Professor of Mechanical Engineering at the University of Kentucky, Paducah Campus. He received his Ph.D. in mechanical engineering from Auburn University in 2015. His primary research areas are thermal management of high-power electronics through jet impingement and thermal characterization of advanced materials used in aerospace and electronics cooling applications. He may be contacted at **john.maddox@uky.edu**.

System Level Thermal Management

- Youngsang Cho, Heonwoo Kim, Kyoungmin Lee, Yunhyeok Im, Heeseok Lee, and Minkyu Kim "Thermal Aware Floorplan Optimization of SOC in Mobile Phone," Samsung Electronics Co.

Mechanics and Reliability

- Pranay P. Nagrani, Ritwik V. Kulkarni & Amy M. Marconnet, "Influence of Thermal Cycling on Degradation Behavior of Thermal Greases," Purdue University.

Emerging Technologies & Fundamentals

- Qian Qian (Purdue University), Xin Zhang (IBM Research), Shurong Tian (IBM Research), Justin A. Weibel (Purdue University), Liang Pan (Purdue University), "Experimental investigation of ultra-thin microchannel oscillating heat pipes with submillimeter-scale thickness," Purdue University.

Best Paper – Runner Up

Component Level Thermal Management

- G. Elsinger (KU Leuven / imec), H. Oprins, V. Cherman (imec), G. Van der Plas (imec), E. Beyne (imec) & I. De Wolf (KU Leuven / imec), "Micro-Scale Jet Cooling: A Numerical Study on Improvement Options."

System Level Thermal Management

- Christopher D. Kim, Allison M. Orr and Amelia A. Cherian, "Bi-Modal Thermal Design of a Spacebourne Rotorcraft Avionics Unit," Johns Hopkins Applied Physics Lab.

Mechanics and Reliability

- Sai Sanjit Ganti, Ganesh Subbarayan, "Multiscale, Non-Intrusive Computational Framework for Analyzing Rate-Dependent Deformation of Solder Joints," Purdue University.

Emerging Technologies & Fundamentals

- Juvani Downer, Mehdi Kabir, Jiajun Xu, "The Design and Development of a Smart Multilayer Coating with Variable Emissivity Capability for Space Vehicle Thermal Control Systems," University of the District of Columbia.

Student Poster and Networking Session

The student poster and networking session provided an opportunity for students to interact with industry and academic leaders in their fields. This venue enabled students to connect with possible future employers and to receive feedback on their work. The student posters were subjected to two rounds of judging based on technical merit, clarity, self-sufficiency of the content, originality of the work, visual presentation, and oral presentation with best and outstanding posters selected for each technical track and one poster was selected as the best overall.

Best Overall Poster

- Diego Vaca, Georgia Institute of Technology "Temperature Dependent Thermal Properties of Thin Film Hafnium Oxide"

Best Posters

Component Level Thermal Management

- Carol Caceres, Villanova University "Dynamic Modeling of a Refrigerant-Based Cross-flow Heat Exchanger for Close-Coupled Hybrid Cooled Data Centers"

System Level Thermal Management

- Falak Mandali, Purdue University "Control Co-Design of a Thermal Management System with Integrated Latent Thermal Energy Storage and a Logic-based Controller"

Mechanics and Reliability

- Pranay Nagrani, Purdue University "Influence of Thermal Cycling on Degradation Behavior of Thermal Greases"

Emerging Technologies & Fundamentals

- Diego Vaca , Georgia Institute of Technology "Temperature Dependent Thermal Properties of Thin Film Hafnium Oxide"

Outstanding Posters

Component Level Thermal Management

- Georg Elsinger, KU Leuven “Micro-Scale Jet Cooling: A Numerical Study on Improvement Options”

System Level Thermal Management

- Joshua Palumbo, University of Toronto “Implementation of a Topologically Optimized Heat Sink for Non-Uniform Heat Fluxes in an EV Fast-Charger”

Mechanics and Reliability

- Jinesh Narangaparambil, Auburn University “Influence of Component Interconnect with Printed Copper Circuits on Realized Mechanical and Electrical Characteristics in FHE Applications”

Emerging Technologies & Fundamentals

- Aalok Gaitonde, Purdue University “Feasibility Assessment of Metrologies for Thermal Resistance Characterization of Deeply Buried Interfaces between Bonded Silicon Layers”

Student Heat Sink Design Challenge

The ASME K-16/IEEE EPS Student Design Challenge is a team competition in which students design, analyze, and optimize an additively manufactured, aluminum heat sinks to cool a constant heat flux power electronics module subject to forced convection. Designs were submitted by teams from around the world and evaluated by a team of experts based on a series of design and manufacturing criteria. For the 2023 competition, the top 4 most effective and creative designs were printed using additive manufacturing facilities at GE and tested using state-of-the-art test equipment at the Southern University of Denmark. The 4 semi-finalist heat sinks are shown in *Figure 1*.

Figure 1: Heat sink design challenge semi-finalists. [Top row left to right: University of North Alabama, Texas A&M University; Bottom row left to right: Technische Universität Berlin, University of Utah]

Winner

- Preston Bodily, Taylor Cox, Chandler Elliott, Zach Julien, Xander Lehnardt, University of Utah (*Figure 2*)

Runner-up

- Kai Wei, Marshall Allen, Mark Luke, Texas A&M University (*Figure 3*)

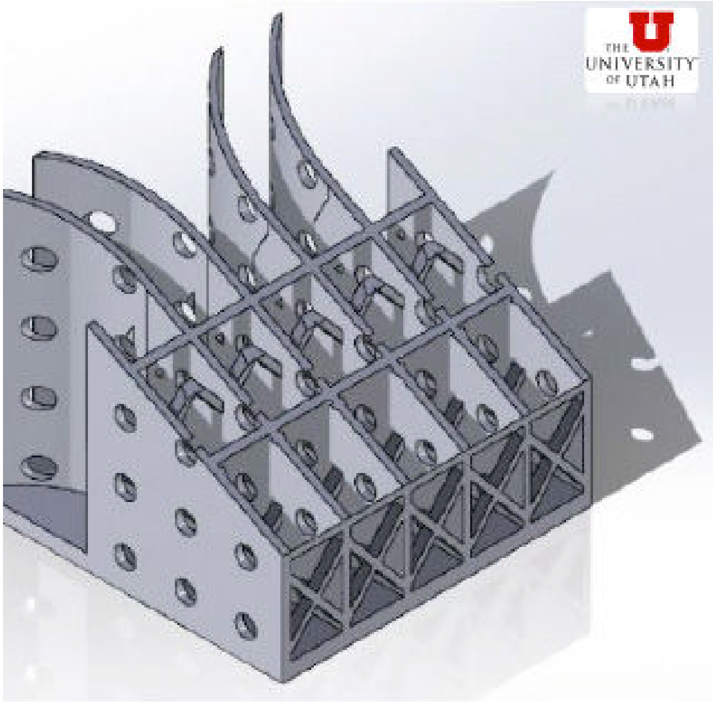


Figure 2: Winning Design – University of Utah

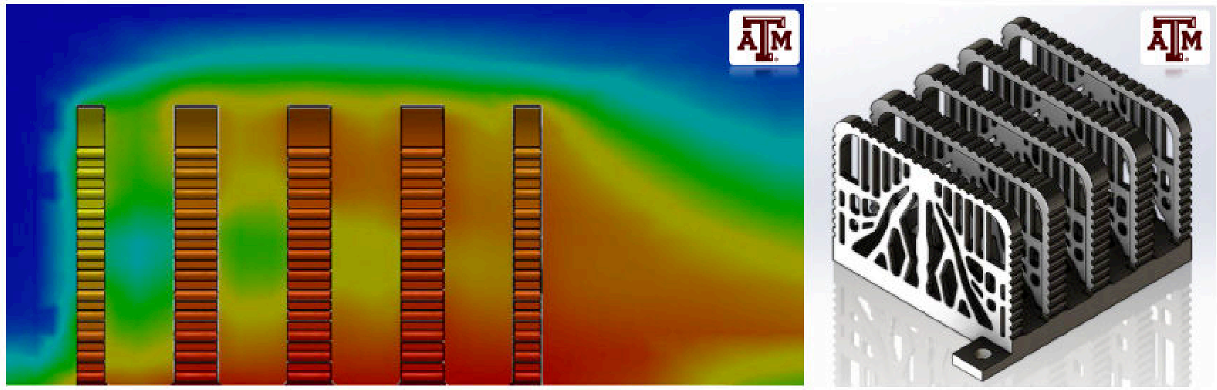


Figure 3: Runner-up – Texas A&M University

Richard Chu ITherm Award for Excellence

Prof. Suresh K. Sitaraman was awarded the Richard Chu ITherm Award for Excellence. Prof. Sitaraman is the Director for the Flexible and Wearable Electronics Advanced Research (FlexWEAR@Tech) Program and the Director for the Computer-Aided Simulation of Packaging Reliability (CASPaR) Lab at Georgia Tech. His expertise is in the areas of fabrication, characterization, physics-based modeling, and thermal-mechanical and reliable design of nano-scale and micro-scale structures for a wide range of applications. Dr. Sitaraman has co-authored more than 340 journal and conference publications in these areas. He has managed several research and development projects funded by US federal agencies, industry, and other sources totaling millions of dollars, and has mentored a vast array of post-doctoral fellows as well as doctoral, master's, bachelor's, and high-school students. Prior to joining Georgia Tech in 1995, Dr. Sitaraman was with IBM Corp.

Proceedings

We are also pleased to announce that the ITherm 2023 Proceedings are available through IEEE Xplore Digital Library at https://ieeexplore.ieee.org/xpl/conhome/10177286/proceeding. Papers appearing in the Table of Contents are available for access and download, along with listings of our Keynote Speakers, Tech Talks, Panels, Sponsors, and Exhibitors.

Sponsors and Exhibitors

ITherm 2023 was made possible by those of you who attended and by the generous support of our sponsors and exhibitors.

ITherm 2023 Organization Committee

Satish Kumar, Ph.D.
Georgia Tech
Program Chair

Ashish Gupta, Ph.D.
Intel Corporation
Vice Program Chair

Amy Marconnet, Ph.D.
Purdue University
Communications Chair

Milnes David, Ph.D.
IBM Corporation
Communications Chair

ITherm 2024

We hope you will join us at the Gaylord Rockies Resort & Convention Center, May 28th-31st, 2024, for ITherm 2024.

ITherm
DENVER, CO
2024

Report About the THERMINIC 2023 Workshop

Marta Rencz, Andras Poppe, and Genevieve Martin

The 29th issue of the THERMINIC (Thermal investigations of ICs and Systems) workshops was held on 27-29 September 2023 in Budapest, Hungary at the Budapest Marriott Hotel. Over 110 participants enjoyed the high quality presentations from 17 countries. About half of the participants came from the industry, half from the academia. This year's major subject of the workshop was **Testing and cooling solutions for power electronics**.

Each day of the workshop was dedicated to a special theme and started with a keynote presentation given by industrial leaders, introducing the major subject of the day.

The first day's papers dealing with thermal management and cooling solutions were presented and discussed in 2 oral and one interactive (poster) sessions. In addition, a vendor session introduced the industrial sponsor's (Siemens, Bosch, Nanotest, Huawei) activities and offerings related to thermal management.

The first day's keynote talk came from Bosch Hungary, given by Szilárd Szőke, with the title of **"In Pursuit of Accuracy: Thermal Design Verification in Automotive Power Electronics"**. It discussed the increased importance of thermal testing in various branches of automotive power electronics and the interplay of reliable thermal tests and thermal simulation, both being part of the same product development workflow.

The second day was dedicated to coupled field modelling and simulation. **"Making Digital Twin Work"** was the title of day 2 keynote talk, given by Prof. G. Q. Zhang from the Delft University of Technology, The Netherlands, who is currently secretary-general of the IEEE International Technology Roadmap of Wide bandgap power semiconductors (ITRW). In his talk he presented the new challenges set by the European Chips Act, and gave an insight into the most burning questions of multi-level heterogeneous system integration and packaging. Prof. Zhang's talk was closely related to two European research projects, PowerizeD – dealing with testing, modelling and lifetime prognostics issues of power electronics components (issues discussed during day 1 of the workshop), and AI-TWILIGHT – a project addressing similar topics in connection with LED based products, that were addressed in much details in a special session on the third day of the workshop.

On the second day the oral sessions discussed the **Optimization, numerical analysis, machine learning** questions of thermal design, followed by a session discussing the **Advances in data processing of thermal transients and compact modelling** and a session discussing **New concepts for data center cooling**.

The third day was dedicated to the thermal issues of solid state lighting devices and systems. The day's keynote talk, **"Challenges and Opportunities to Improve the Performance of LED Lighting"** was presented by Dr László Balázs, a leading expert of horticultural lighting, from the Hungarian University of Agriculture and Life Sciences who formerly has been working in the lighting industry for about two decades.

The first part of the day was dedicated to presenting the results of the AI-TWILIGHT (AI powered digital twin generation for the lighting industry) H2020 ECSEL project of the EU. The two oral sessions:

AI-TWILIGHT Session 1: Thermal, optical and power cycling testing and modelling of LED packages and **AI-TWILIGHT Session 2: Modelling of LEDs** presented the results achieved in the first 2 years at the different project partners. The morning was closed with other oral presentations within the subject of **Thermal investigation of LEDs and PV cells**.

In the afternoon a session with papers in the field of **Thermal & reliability testing** was closing the technical presentations.

The workshop was closed by announcing the best paper, the best poster and best young researcher awards to the presenters. The diplomas were accompanied with valuable gifts: the newest pieces of electronics were offered to the winners by Huawei.

Nils J. Ziegler received the Best Paper Award from Vadim Tsoi (Huawei)

The Best Young Researcher Award went to David Walther from Chemnitz University of Technology

The Best Poster was awarded to Artur Jurkowski (right) and Marcin Wójcik.
In the background András Poppe, the Therminic 2023 Programme Chair

SPONSORED BY:

IEEE

THERMINIC 2024

The **30th THERMINIC Workshop** will be held in Toulouse, France, September 25 – 27, 2024. THERMINIC is the major EuropeanWorkshop related to thermal and reliability issues in electronic components and systems. For academics and industrialists involved in micro and power electronics this annual event promises to be a very special occasion with a high quality technical program and exciting social events. We invite delegates to consider submitting abstracts that are related, but not limited to, the following topics:

- Thermal Phenomena in Simulation & Experiment
- Electronics Cooling Concepts & Applications
- Thermo-Mechanical Reliability

Work targeting aeronautics and space will be particularly appreciated.

Deadline abstract submission: April 5, 2024
Notification of acceptance: June 13, 2024
Submission of paper for workshop proceedings: August 7, 2024
Website: **https://therminic2024.eu/**

Therminic2024 Organization Committee

Jean-Pierre Fradin
Icam, Toulouse Campus,
France
Head of Research

Patrick Tounsi
INSA Toulouse,
Computer and Electrical
Engineering Department
and Research at the
LAAS-CNRS

Call for Authors and Contributors!

Want to be a part of the next issue of Electronics Cooling? Have an article or blog post you'd like to write for Electronics-Cooling.com?

Let us know at
editor@electronics-cooling.com

electronics
COOLING
www.Electronics-Cooling.com

Index of ADVERTISERS

Electronics Cooling
716 Dekalb Pike, #351
Blue Bell, PA 19422

t: (484) 688-0300
e: info@electronics-cooling.com
w: www.electronics-cooling.com
page: 32

Ellsworth Adhesives
W129 N10825 Washington Drive
Germantown, WI 53022

t: (877) 454-9224
e: info@ellsworth.com
w: www.ellsworth.com
page: 2

Lectrix
716 Dekalb Pike, #351
Blue Bell, PA 19422

t: (484) 688-0300
e: info@lectrixgroup.com
w: www.lectrixgroup.com
page: 34

SEMI-THERM
3287 Kifer Road
Santa Clara, CA 95051

t: (408) 840-2354
w: www.semi-therm.org
page: 6