SUMMER 2024
electronics-cooling.com

electronics COOLING

FEATURED IN THIS EDITION

CONTENTS

electronics COOLING
electronics-cooling.com

PUBLISHED BY
Lectrix
716 Dekalb Pike, #351
Blue Bell, PA 19422
Phone: +1 484-688-0300
info@lectrixgroup.com
lectrixgroup.com

CHIEF EXECUTIVE OFFICER
Graham Kilshaw | graham@lectrixgroup.com

DIRECTOR OF BUSINESS DEVELOPMENT
Ashlee Zapata-McCants | ashlee@lectrixgroup.com

CREATIVE DIRECTOR
Kate Teti | kate@lectrixgroup.com

GRAPHIC DESIGNER
Marcos Cruz | marcos@lectrixgroup.com

DELIVERY MANAGER
Mackenzie Mann | mackenzie@lectrixgroup.com

▶**SUBSCRIPTIONS ONLINE**
at electronics-cooling.com

For subscription changes email
info@electronics-cooling.com

FREE SUBSCRIPTIONS

Lectrix®, Electronics Cooling®—The **2024 Summer Edition** is distributed digitally at no charge to engineers and managers engaged in the application, selection, design, test, specification or procurement of electronic components, systems, materials, equipment, facilities or related fabrication services. Subscriptions are available through electronics-cooling.com.

LECTRIX®

EDITORIAL

Victor Chiriac
Associate Technical Editor of *Electronics Cooling Magazine*
Co-founder and Managing Partner, Global Cooling Technology Group

Dear *Electronics Cooling Magazine* readers, we welcome you to the Summer 2024 edition of our publication. We are happy to share with our readership articles spanning from impingement cooling to good general practices in the thermal engineering field, to mechanical challenges and opportunities.

As I've done in the past few years, I am starting this editorial with a review of the most advanced technology landscapes that continue to shape our world. A brief review of the CES (Consumer Electronics Show) event in Las Vegas is always on top of my editorial agenda. The technology advancements are always related to higher thermal management needs, thus the significant interest and impact that this poses for our electronics cooling community.

CES 2024 showcased cutting-edge technology and innovative products from a range of industries, including automotive, smart home, health, wellness and more. The event highlighted the continued advancement of artificial intelligence (AI), virtual reality and 5G technology. Key themes included sustainability, connectivity, and the future of transportation. Attendees were able to see the latest advancements in consumer electronics and experience interactive demonstrations. Overall, CES 2024 was a showcase of the exciting possibilities and potential for the future of technology.

The advancements of AI at CES 2024 included:

1) Advanced AI-driven robots: Companies demonstrating robots equipped with sophisticated AI capabilities, such as autonomous navigation, natural language processing, and the ability to perform complex tasks. These robots were designed for a variety of purposes, including customer service, healthcare, and domestic assistance.
2) AI-powered smart home devices: Smart home devices integrated with AI technology were a prominent feature at CES 2024. These devices were able to learn and to adapt to users' preferences, anticipate their needs, and to provide personalized recommendations for energy efficiency, security, and comfort.
3) AI-infused automotive technologies: Car manufacturers showcased advanced AI features in their vehicles, such as autonomous driving systems, predictive maintenance capabilities, and personalized in-car experiences. AI was used to enhance safety, improve efficiency, and create a seamless driving experience, and
4) AI-driven health solutions.

At CES 2024, there were several advancements in 5G technology and connectivity, including:

1) 5G -enabled devices: many companies showcased a wide range of devices, including smartphones, tablets, laptops and IoT devices, equipped with 5G connectivity. These devices demonstrated faster speeds, lower latency, and improved network reliability, enabling enhanced user experiences and more efficient data transmission.
2) 5G infrastructure and network capabilities: Telecommunication companies and infrastructure providers showcased advancements in 5G network technology, including increased coverage, capacity and efficiency. They presented innovations in small cell deployment, network slicing, and edge computing to support the growing demand for high-speed, low-latency connectivity.
3) Smart city solutions: Smart city initiatives highlighted the impact of 5G on urban environments, with demonstrations of connected infrastructure, smart transportation systems, and IoT sensors enabled by high speed 5G networks. These solutions aimed to improve efficiency, sustainability, and quality of life in urban areas.

As shown, all these advanced technologies require dedicated and novel thermal solutions that fit within thinner, smaller devices (for the mobile space) of much larger heat loads (for the data center and large-scale compute applications). The traditional air-cooling solutions are slowly being replaced by the liquid and two-phase (refrigeration) cooling solutions with new form factors and shapes.

We always encourage our readership to contact us with materials to be published. We are always seeking great ideas and teaching fundamentals to our thermal community of both young and seasoned engineers. Please consider summarizing your thoughts and work on novel cooling solutions and challenging methodologies that enable AI, 5G/6G and other advanced technologies that move our society to the next level!

Thank you, and I close my thoughts by wishing you all a great year 2024, with many accomplishments and success!

TECHNICAL EDITORS SPOTLIGHT

Meet the 2024 Editorial Board

VICTOR CHIRIAC, PhD | GLOBAL COOLING TECHNOLOGY GROUP

Associate Technical Editor

A fellow of the American Society of Mechanical Engineers (ASME) since 2014, Dr. Victor Adrian Chiriac is a co-founder and a managing partner with the Global Cooling Technology Group since 2019. He previously held technology/engineering leadership roles with Motorola (1999-2010), Qualcomm (2010 – 2018) and Huawei R&D USA (2018 – 2019). Dr. Chiriac was elected Chair of the ASME K-16 Electronics Cooling Committee and was elected the Arizona and New Mexico IMAPS Chapter President. He is a leading member of the organizing committees of ASME/InterPack, ASME/ IMECE and IEEE/CPMT Itherm Conferences. He holds 21 U.S. issued patents, 2 US Trade Secrets and 1 Defensive Publication (with Motorola), and has published over 110 papers in scientific journals and at conferences.

► vchiriac@gctg-llc.com

GENEVIEVE MARTIN | ASML

Associate Technical Editor

Genevieve Martin is a Senior Group Manager with ASML in the Netherlands. She has worked in the field of cooling of electronics and thermal management for over twenty years in different application fields. From 2016 to 2019, she coordinated the European project Delphi4LED, which dealt with multi-domain compact modeling of LEDs and, since 2021, is coordinating the AI-TWILIGHT project. She served as general chair of the SEMI-THERM conference and is an active reviewer and technical committee member in key conferences including SEMI-THERM, Therminic, and Eurosime. She has over 20 journal and conference papers and 16 worldwide patents.

► gmartin.sig1@gmail.com

ALEX OCKFEN, P.E. | META

Associate Technical Editor

Alex Ockfen is a product design engineer at Meta (formerly Facebook), providing technical leadership for thermal and structural design of consumer electronics products. He held previous positions at Raytheon where he obtained experience in thermal management and electronics cooling of a wide range of aerospace and defense applications. He has more than 10 journal and conference publications, is an inventor on multiple patents, is a professional mechanical engineer, and is currently serving as program chair of the SEMI-THERM conference.

► alex.ockfen@meta.com

ROSS WILCOXON | COLLINS AEROSPACE

Associate Technical Editor

Dr. Ross Wilcoxon is a Senior Technical Fellow in the Collins Aerospace Advanced Technology group. He conducts research and supports product development in the areas of component reliability, electronics packaging, and thermal management for communication, processing, displays, and radars. He has more than 40 journal and conference publications and is an inventor on more than 30 US Patents. Prior to joining Rockwell Collins (now Collins Aerospace) in 1998, he was an assistant professor at South Dakota State University.

► ross.wilcoxon@collins.com

COOLING EVENTS

News of Upcoming 2024 Thermal Management Events

JUL
4-5

ICEHTFMT 2024

Four Points by Sheraton Catania Hotel & Conference Center | Prague, Czechia

The International Conference on Experimental Heat Transfer, Fluid Mechanics and Thermodynamics aims to bring together leading academic scientists, researchers and research scholars to exchange and share their experiences and research results on all aspects of Experimental Heat Transfer, Fluid Mechanics and Thermodynamics. It also provides a premier interdisciplinary platform for researchers, practitioners and educators to present and discuss the most recent innovations, trends, and concerns as well as practical challenges encountered and solutions adopted in the fields of Experimental Heat Transfer, Fluid Mechanics and Thermodynamics. With its high quality, it provides an exceptional value for students, academics and industry researchers.

► **waset.org/experimental-heat-transfer-fluid-mechanics-and-thermodynamics-conference-in-july-2024-in-prague**

AUG
26-30

ExHFT-10

Rodos Palace | Rhodes, Greece

The 10th World Conference on Experimental Heat Transfer, Fluid Mechanics and Thermodynamics (ExHFT-10) goal is to set up an international forum of researchers from industry and, academia where new research ideas, advanced methods, sophisticated instrumentation and thoughtful results are presented on heat transfer, fluid mechanics and thermodynamics. Apart from bringing together the well-established community in the field, ExHFT-10 has the ambition to attract also young researchers who will not only report their work to a knowledgeable audience, but they will also communicate present-day science and engineering problems in an effort to identify possible answers to their early career questions.

► **exhft-10.gr**

SEP
25-27

THERMINIC 2024

Suburban Collection Showplace | Toulouse, France

THERMINIC is the major European Workshop related to thermal and reliability issues in electronic components and systems. For aca- demics and industrialists involved in micro and power electronics this annual event promises to be a very special occasion with a high quality technical programme and exciting social events.

► **therminic2024.eu**

Thermocouple Attachment

Ross Wilcoxon
Associate Technical Editor for *Electronics Cooling*
Collins Aerospace

The previous article in this series on thermocouples described how the size of the thermocouple wire could affect its accuracy [1]. This is particularly true if the wire is exposed to high convection coefficients. This article addresses a separate issue, namely the degree to which the attachment method impacts thermocouple readings. As it turns out, once again the convection conditions used in testing will influence the degree to which the attachment method can affect measurements.

Various researchers have reported the impact of thermocouple attachment on measurement accuracy. For example, an experimental investigation of component temperatures with different thermocouple types, sizes and attachment methods (copper tape and epoxy) [2]. That study found only a 3% reduction in the measured thermal resistance of the part when copper tape was used rather than epoxy. In comparison, using a larger (30-gauge) type T thermocouple led to ~11% error in the thermal resistance measurement compared to a smaller (36-gauge) Type J thermocouple. In another example of relevant work, a detailed numerical study investigated a wide range of factors that affect thermocouple accuracy [3]. This included the effects of thermocouple type, size, cooling air conditions, and how the thickness and thermal conductivity of the epoxy used to attach the thermocouple to a surface affected the measurement. Their results, for a specific set of external boundary conditions, showed that epoxy bond lines of more than 1 mm could lead to temperature measurement errors of over 30%. The thermal conductivity of the epoxy was also shown to affect the measured temperature by ~5-10% depending on the wire size. Alternatively, mechanical attachment methods such as peening and crimping, can be used to place thermocouples on a surface [4].

For this article, a test was conducted by attaching type T, 30-gauge thermocouples to an aluminum plate using four different methods, as shown in *Figure 1*. The four inset images on this figure illustrate the four attachment methods. Inset *figure 1a)* shows the thermocouple attached using a standard two-part epoxy. *Figure 1b)* shows a thermocouple held to the aluminum plate with an adhesive tape. *Figure 1c)* shows a thermocouple attached to the plate using a fast-curing cyanoacrylate adhesive, i.e., a 'Super glue'. Finally *Figure 1d)* shows a thermocouple attached with the same two-part epoxy as in *Figure 1a)*, but with a thicker bond line. As can be seen in the image of the full plate, large paper clips (with wire diameter of ~1mm) were placed on the plate so that the thermocouple beads were suspended above it to assess how much the larger stand-off

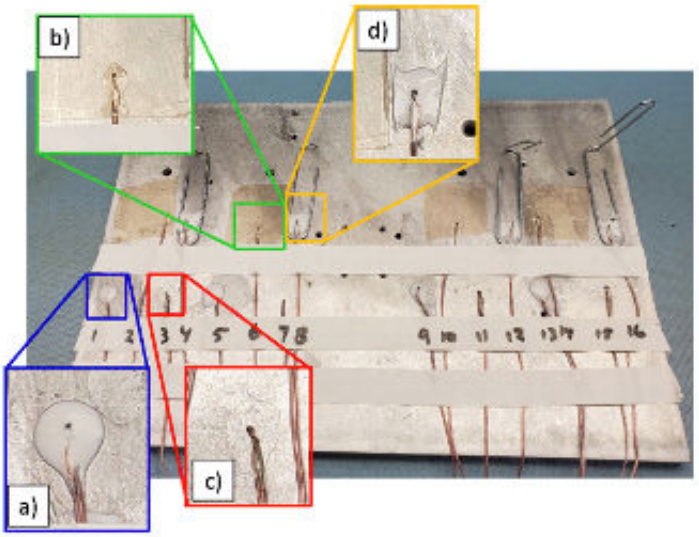


Figure 1: Test Fixture for Different Thermocouple Attachment Methods

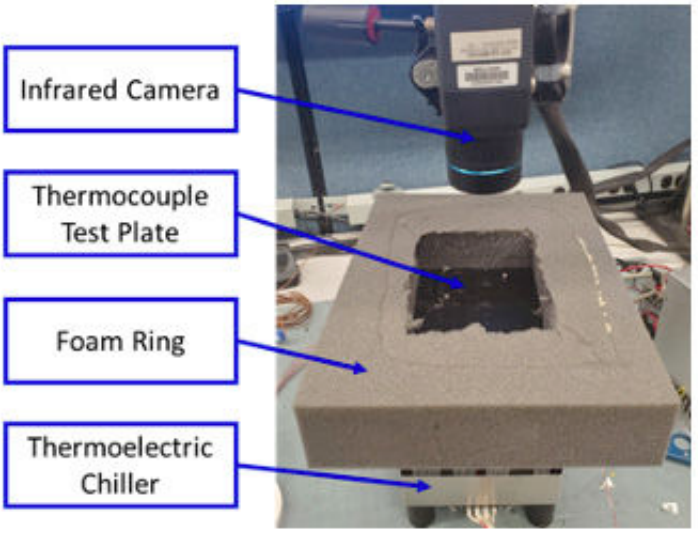


Figure 2: Thermocouple Test Setup

affects result. Then the epoxy was applied and, after the epoxy had cured, the paper clips were removed. Note that the paper clip are still present in the picture of the full plate but removed for the inset picture d). Four replicates of each attachment approach were included on the plate with, for example, thermocouples 1, 5, 9, and 13 attached with the conventional approach using two-part epoxy illustrated in *Figure 1a)*.

After the epoxy had cured, the aluminum plate was painted so that its emissivity was relatively uniform across the entire area. It was then attached to a thermoelectric cooler that maintained the plate temperature at controlled temperatures. The plate temperature was monitored using an infrared camera, as shown in *Figure 2*. Lab ambient temperature during this testing was ~20°C.

Since initial testing showed that the temperatures were affected by the surrounding conditions, tests were conducted using three different boundary conditions to compare effects. In the 'Blowing Air' condition, the plate with the thermocouples was exposed to moderate air flow (~3-4 m/s) from a small fan that was ~1 m away. *Figure 2* shows the 'Still Air' configuration, in which the fan was turned off and a foam ring was placed on the plate to limit heat transfer from the plate to natural convection and radiation. For the 'Covered' configuration, an opaque foam cover was placed on top of the foam ring and the system was allowed to stabilize with minimal convection or radiation from the test plate. Then the cover was removed, and the IR and thermocouple temperatures were quickly collected before the system could respond to the modified boundary condition.

These measurements were done for four different nominal plate temperatures as measured with the IR imager. Test results are shown in *Figure 3*.

The images in *Figure 3* show the measurement error of the thermocouples relative to the average temperature of the plate. In these

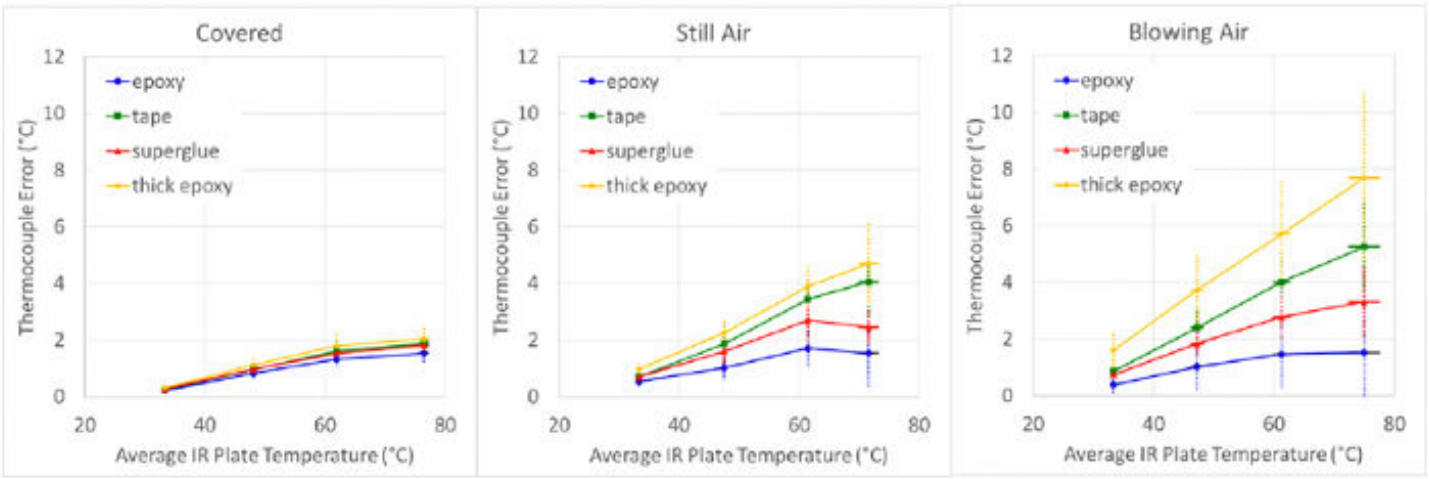


Figure 3: Temperature Differences for Different Thermocouple Attachment Methods

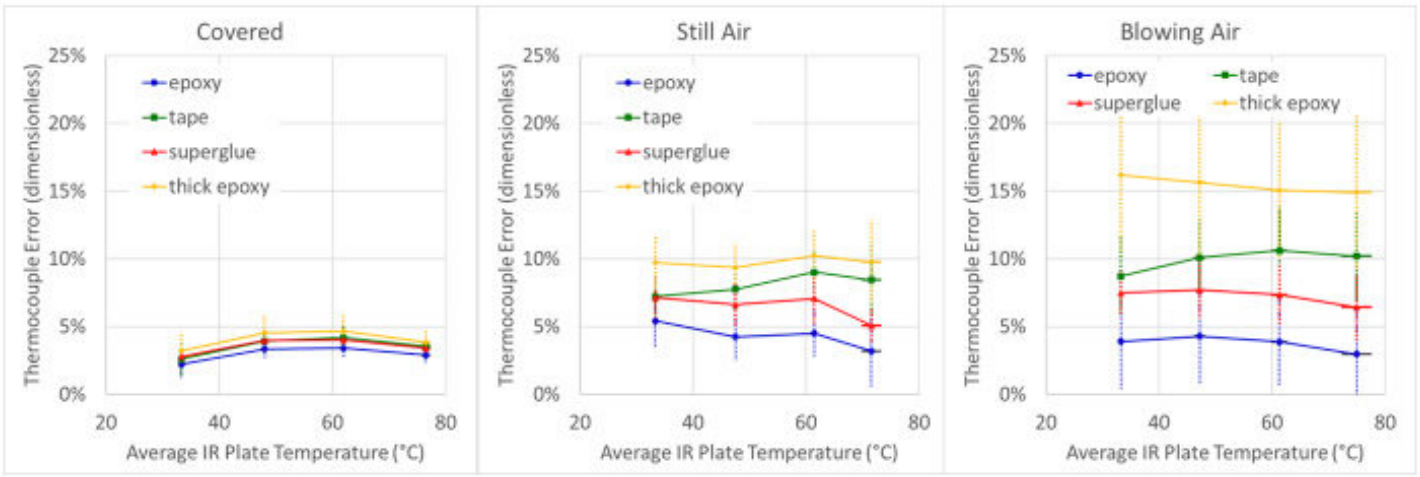


Figure 4: Normalized Temperature Differences for Different Thermocouple Attachment Methods

plots, the error corresponds to the average plate temperature minus the thermocouple measurement, i.e., the thermocouple measurements were always lower than the plate temperatures. Uncertainty bars indicate one standard deviations of the four samples of each attachment method. These data show that, when the plate was covered to minimize heat transfer from its top surface, the four attachment methods produced similar results with ~2°C error when the plate was at ~75°C. However, when the thermocouples were exposed to blowing air, there were substantial differences in the measurement error depending on the attachment method. The thick epoxy had the most significant difference with average offset values of ~8°C at the highest plate temperature. The still air conditions led to less measurement error than blowing air, but the thick epoxy did generate over 4°C error. In each case, the thermocouples with normal epoxy had approximately the same error value, regardless of the boundary conditions.

Figure 4 shows the same data as *Figure 3*, but the measurement difference is normalized by the temperature rise above ambient temperature[1]. These results show generally flat lines, which indicate that the relative error for a given attachment method may be constant for a given boundary condition.

Summary

While this testing was relatively crude, it does illustrate that the method used to attach the thermocouple can influence its accuracy. But the degree to which the attachment material affects the results does depend on the test conditions. If the heat transfer through the attachment material is minimized, by insulating the top surface, then the measurement error associated with the attachment method is relatively small. However, if a thermocouple is attached to a surface that is cooled by blowing air or flowing liquid, the conductive thermal resistance through the layer of attachment material will lead to measurement error. The magnitude of this error increases with thicker and lower conductivity attachment.

[1] $T_{normalized}=(T_{IR}-T_{thermocouple})/(T_{IR}-T_{ambient})$

References

[1] R. Wilcoxon, “Tech Brief - Effect of Thermocouple Size”, Electronics Cooling Magazine, Spring 2024 Issue, pp 9 – 11, https://www.electronics-cooling.com/2024/03/tech-brief-effect-of-thermocouple-size/

[2] G. E. Tan, C. Carte and Y. Fan, "Thermocouple Attachment Methodology for Memory," 2021 20th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (iTherm), San Diego, CA, USA, 2021, pp. 1150-1153

[3] Q. He, S. Smith and G. Xiong, "Thermocouple attachment using epoxy in electronic system thermal measurements — A numerical experiment," 2011 27th Annual IEEE Semiconductor Thermal Measurement and Management Symposium, San Jose, CA, USA, 2011, pp. 280-291

[4] Attaching Thermocouples by Peening or Crimping”, NASA Tech Briefs, March 1, 2006, https://www.techbriefs.com/component/content/article/1529-ksc-12775

Radiation Basics: When Does it Matter?

Alex Ockfen
Associate Technical Editor for *Electronics Cooling*
Product Design Engineer at Meta

Introduction

This is the first installment in a series of articles that aim to explore a range of practical topics on radiation that will be relevant to those of us focused on electronics cooling and thermal design.

While radiation is one of the three fundamental modes of heat transfer, it is often the last topic covered in an introductory heat transfer course. This may leave some of us intimidated when we look back at the complicated equations, try and remember the various definitions, decode the underlying assumptions, etc. I hope to bring some clarity to these common radiation questions here.
Let's start with the most basic question. When do we need to consider radiation in thermal design, and when can it be reasonably neglected? Understanding this is useful because radiation is a complex phenomenon, introduces non-linearities, and can be computationally expensive to calculate (e.g., non-linear, view factors, ray tracing, etc.).

The Basics

For a gray body, the net heat crossing the surface of the body is defined by *equation 1*; where Q is the heat rate in Watts, ε_{12} is the effective emissivity between the surface and an interacting body, F_{12} is the view factor between the surface and a interacting body, A is the surface area, σ is the Stefan Boltzmann constant (5.67e-8 W/m^2-K^4), T_s is the surface temperature of the body in K, and T_∞ is the temperature of the interacting body in K.

$$Q = \varepsilon_{12} F_{12} A \sigma (T_s^4 - T_\infty^4) \qquad [1]$$

Inspection of this equation identifies the key factors influencing radiative transfer. The emissivity, view factor and surface area represent linear design 'knobs' that influence heat rate. The temperature term is non-linear and increases to the 4th power.

Given that conduction and convection are linear functions of the temperature difference, it is also often convenient to reformulate the radiation equation into the linearized format provided by *equations 2* and *3*, where h_r is a linearized radiation heat transfer coefficient.

$$Q = h_r A (T_s - T_\infty) \qquad [2]$$

$$h_r = \varepsilon_{12} F_{12} \sigma (T_s + T_\infty)(T_s^2 + T_\infty^2) \qquad [3]$$

For the purposes of this study, we will assume that the surface of interest interacts with a blackbody (ε =1) that fully surrounds it (F_{12}=1). This approximates a surface that is radiating to a uniform environment, simplifying *equation 3* to *equation 4*. See reference [5] for additional information on the derivation of this equation.

$$h_r = \varepsilon \sigma (T_s + T_\infty)(T_s^2 + T_\infty^2) \qquad [4]$$

These equations now equip us with the tools needed to quantify the importance of radiation across common thermal applications.

Natural Convection Environments

Let's start by quantifying when radiation is important in natural convection environments. Natural convection environments are common for passively cooled devices such as consumer electronics products. The empirical Nusselt correlation for natural convection is re-arranged to provide the convection coefficient (h_c) in *equation 5*, where, Ra is the Rayleigh number, k is the thermal conductivity of fluid medium, and Lc is the characteristic length of the body, and C and n are empirical constants. For the purposes of this article, we will assume a vertical plate with coefficients C and n of 0.59 and 0.25 respectively [1]. However, one can easily plug in different correlations for varying geometries and/or orientations.

$$h_c = C Ra^n \left(\frac{k}{L_c}\right) \qquad [5]$$

The Rayleigh number is calculated with *equation 6*, where g is the acceleration of gravity, β is expansion coefficient, v is kinematic viscosity, and Pr is the Prandtl number.

$$Ra = GrPr = \frac{g\beta L_c^3 (T_s - T_\infty)}{\nu^2} Pr \qquad [6]$$

The heat balance for a device can be calculated by equating its heat generation rate with the sum of the heat rejected by natural convection and radiation as shown in *equation 7*.

$$Q = (h_r + h_c)A(T_s - T_\infty) \qquad [7]$$

For the purposes of determining when radiation matters, it is convenient to equate the natural convection and radiative heat transfer coefficients and solve for one of the common design variables. In this case, we will solve for the emissivity required to match the heat rejected by radiation and natural convection, see *equation 8*.

$$\varepsilon = \frac{C\left(\frac{g\beta L_c^3(T_s - T_\infty)}{\nu^2}Pr\right)^n\left(\frac{k}{L_c}\right)}{\sigma(T_s+T_\infty)(T_s^2+T_\infty^2)} \qquad [8]$$

Although this equation is a function of many variables, the characteristic length and the temperature are of greatest interest because they represent thermal design knobs.

Figure 1 confirms that radiation matters and must be considered in natural convection environments. The emissivities of common external painted surfaces are typically ≥ 0.8. This means that radiation may be the dominant heat rejection mode across device length scales and temperature ranges in natural convection environments. Even for the reasonably low emissivity of 0.2, which may be representative of a polished surface, radiation cannot be ignored.

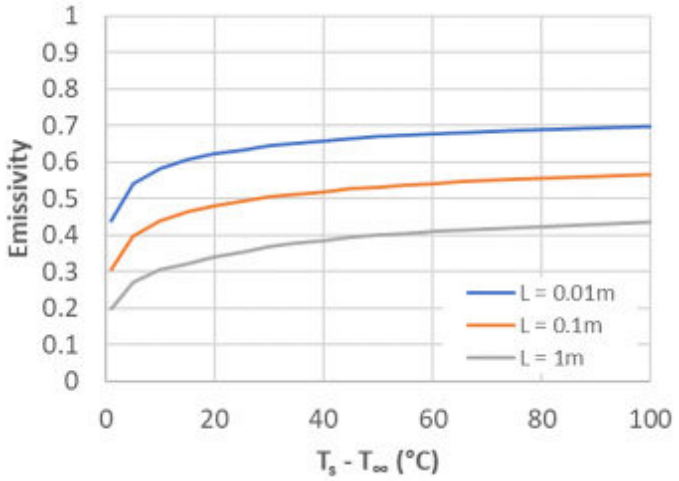


Figure 1: Emissivity required for radiative heat rejection to match natural convection

Forced Convection Environments

Does the importance of radiation extend to forced convection environments? Forced airflow is a common means to actively cool electronics such as laptops or datacenters. It can consist of internally ducted airflow, or external airflow over a product. This airflow may be intentionally applied using a fan or can naturally occur via wind or movement. The empirical correlation for the average external forced convection heat transfer coefficient is provided in *equation 9*, where Re_L is the Reynolds number calculated at the characteristic length, and C, m, A and n are empirical constants. We will assume a flat plate with the coefficients C, m, A and n of 0.037, 0.8, 871 and 0.33 respectively for mixed flow and 0.664, 0.5, 0 and 0.33 for laminar flow, with turbulent transition at a Reynolds number of $5x10^5$ [1]. However, one could similarly expand to other geometries and conditions by considering alternate correlations.

$$h_c = (CRe_L{}^m - A)Pr^n\left(\frac{k}{L_c}\right) \qquad [9]$$

The ratio of the radiative heat rejection to the total heat rejection in forced convection scenarios is illustrated in *Figure 2*. In order to represent typical electronics cooling scenarios, the surface temperature is assumed to be 50°C, the ambient environment is assumed to be 25°C, and the surface emissivity is assumed to be 0.8.

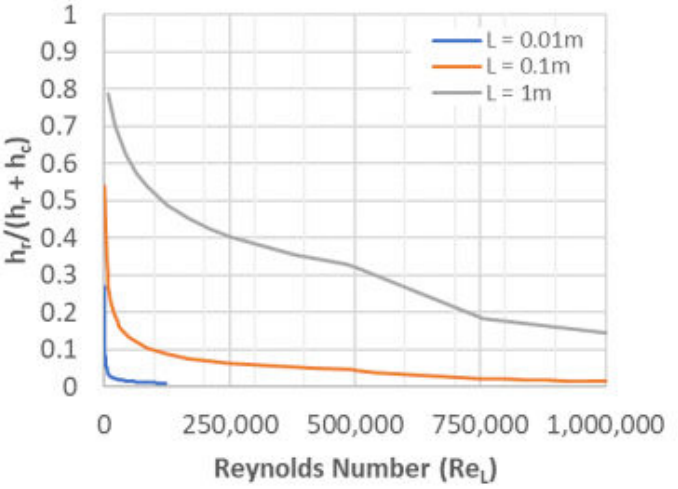


Figure 2: Ratio of radiative heat rejection to total heat rejection for external forced convection environments

Radiation is shown to be important only for small Reynolds numbers (velocities < 5 m/s) or for very large body dimensions. The Reynolds number dependence makes sense, and at very low Reynolds numbers the flow velocities may approach those of natural convection. The non-negligible radiative contribution to cooling of large bodies is due to the increased boundary layer thickness that yields a reduced average convection coefficient. Note that this assumes parallel flow along a flat plate with no obstructions. Flow impingement and complex flow structures typical of complex real-world geometries will generally increase convective mixing and further reduce the effect of radiation. Thus, radiation can often be neglected in electronics cooling with forced convection. However, one should double check when the application includes low velocities or large geometrical dimensions.

Aerodynamic Heating Environments

While it is common for both radiation and convection to represent a means for rejecting heat in many electronics cooling applications, radiation also plays an important role in some less common electronics cooling applications. One such application occurs in high-speed vehicles that experience aerodynamic heating. In these applications, convection can represent a heat source to the electronics.

The convective heat flux is driven by the recovery temperature (T_r) as illustrated in *equation 10*. The recovery temperature is calculated using *equation 11* and is a function of the Mach number (M), the recovery factor (r), and the heat capacity ratio (γ).

$$Q_c = h_c A(T_s - T_r) \qquad [10]$$

$$T_r = T_\infty \left(1 + r\frac{1-\gamma}{2}M^2\right) \qquad [11]$$

When convection acts as a heat source instead of a heat sink, radiation will be a primary means of rejecting heat to cool the electronics. The equilibrium surface temperature of a body experiencing aerodynamic heating can be determined by balancing *equations 1* and *10*, resulting in *equation 12*.

$$\varepsilon\sigma(T_s^4 - T_\infty^4) = h_c\left(T_s - T_\infty\left(1 + r\frac{1-\gamma}{2}M^2\right)\right) \quad [12]$$

This equation can be numerically solved using any "goal seek" method, such as Solver in Excel, to identify the equilibrium temperature the body will reach. This is important to the field of electronics cooling because it sets the heat sink temperature for steady operation in these environments. An example is shown in *Figure 3* for a few different Mach numbers in a 0°C environment. Note that the environment temperature will be a function of the altitude and location of operation. Similarly, the convective heat transfer coefficient will be a function of the altitude, body size, and body velocity. While this example illustrates the general themes only, the reader is referred to a detailed text, such as reference [4], for more information.

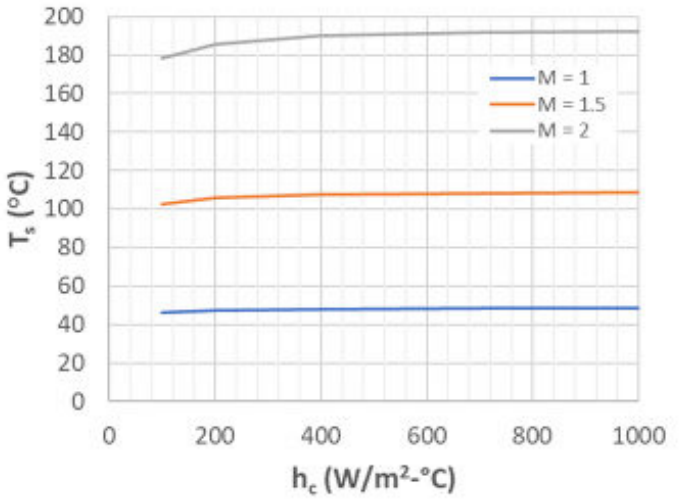


Figure 3: Equilibrium surface temperature for notional aerodynamic application (ε=0.8)

Overall, this example illustrates that radiation can also play a role in setting environmental operating temperatures in some extreme electronics environments. Given the high temperatures that can occur in these conditions, it may (i) justify development of robust electronics that can operate in elevated temperatures, or (ii) drive insulation requirements to ensure electronics aren't damaged during transient exposures.

Space Applications

Lastly, we can't talk about radiation without mentioning operation in vacuum conditions, such as satellites in space. In a vacuum there is no convection, and conduction is largely limited to heat transfer within the device itself. Thus, the primary means of heat transfer between a device and the environment is through radiation [2].

A basic steady-state heat balance is described in *equation 13*, where Q_{elx} represents heat generation by the electronics, $Q_{rad,in}$ represents incoming radiation sources, and $Q_{rad,out}$ represents radiation to space. Incoming radiation sources include solar loading, albedo, and planet shine. Outgoing radiation is rejected to space, a heat sink at ~4K.

$$Q_{elx} + Q_{rad,in} = Q_{rad,out} \qquad [13]$$

Figure 4 quantifies the range of heat flux rejected to space across typical electronics operating temperatures and emissivity values. These values are non-trivial and may rival that of solar loading in some cases (e.g. absorptivity values, orientations). In space applications, there may also be times where this heat rejection can cool electronics below their operating temperatures, requiring additional measures to be taken (e.g. heaters, insulation, orbit control, etc.). The bottom line is that radiation matters in space environments, and the thermal engineer must consider both incoming and outgoing radiation sources.

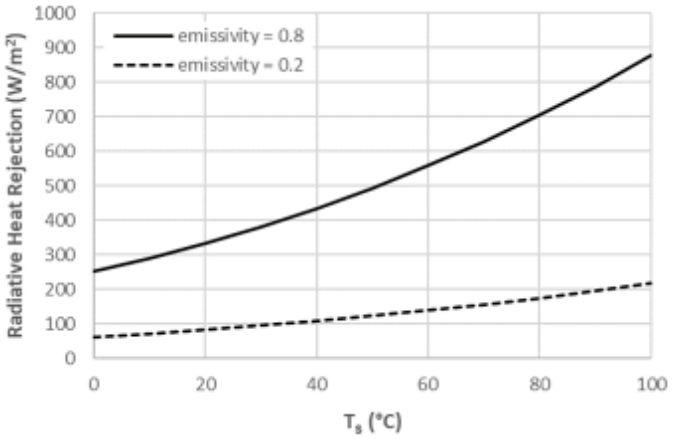


Figure 4: Radiative heat rejection potential to deep space at 4K (for typical electronics operating range)

Concluding Remarks

There is a common misconception that radiation only matters when temperatures are very high. This article challenges that assumption and provides several examples to help the practicing thermal engineer determine when they should account for radiation, or at the very least, when to double check their assumptions

with early hand calculations. The following summary provides a starting point:

- Radiation is significant in natural convection environments and must be considered.
- Radiation is less significant in forced convection environment, but one should double check when velocities are low or geometrical dimensions are large.
- Radiation is the primary means of heat transfer in vacuum environments and must be considered.

References

[1] Frank Incropera and David DeWitt, Fundamentals of Heat and Mass Transfer, 4th Edition, Wiley (1996)

[2] NASA, State of the art of small spacecraft technology: thermal control, https://www.nasa.gov/smallsat-institute/sst-soa/thermal-control/

[3] Bruce Guenin, Don't Underestimate Radiation in Electronics Cooling, https://www.electronics-cooling.com/2001/02/dont-underestimate-radiation-in-electronic-cooling/

[4] Robert Wesley Truitt, Fundamentals of Aerodynamic Heating, Ronald Press Company (1960)

[5] Ross Wilcoxon, A Simple Method for Estimating Radiation Heat Transfer, Electronics Cooling Magazine, Fall 2018

How Many Ways Can Temperature Affect Performance and Reliability of Electronic Systems?

Abhijit Dasgupta
Center for Advanced Life Cycle Engineering, University of Maryland

Thermal management in high performance electronics has become a leading challenge for design and reliability engineers. Harsh temperatures can be caused either by harsh operational conditions (high power dissipation), or by harsh environmental conditions. Both require adequate thermal management to ensure that the product temperature stays within acceptable limits. High temperature, significant cyclic excursions of temperature, strong temperature gradients, and rapid temperature transients, can cause multi-physics degradation to electronic/photonic systems (including components, substrates, and interconnects), leading to progressive aging, degradation of system performance and eventual failure. Multi-physics refers to thermal, chemical, and mechanical aging/degradation mechanisms. 'Systems' includes components, substrates, and interconnects.

Modern electronic systems consist of complex multiscale (nanoscale-to-macroscale) features. A typical integrated circuit (IC) component may utilize heterogeneous integration (HI) technology (*Figure 1a*). typical HI architecture contains a diverse set of co-packaged dies that perform multiple functions, such as digital ICs (of diverse nodes) for computing and memory, analog and RF ICs, silicon-photonics ICs, wide band-gap (WBG) power ICs, MEMS sensor ICs, etc. As shown in *Figure 1b*, typically, these ICs could be arranged in 2.5D or 3D stacked configurations on/in silicon or glass or organic interposers and substrates and interconnected with bridges, microbump and C4 solder joints, copper-bump hybrid joints and wire bonds. There are typically many ultra-dense layers of metal traces and through-thickness vias in the BEOL (Back-end-of-the-line) and RDL (redistribution layers) of individual chips/substrates. The substrate/interposer usually also contains numerous surface-mounted or embedded passive components. 3D die-stacking often creates novel challenges for getting the heat out, such as requiring advanced microchannel multi-phase cooling solutions. Such HI advanced packages typically use a wide variety of highly engineered material systems (and corresponding interfaces): doped semiconductors, complex metal alloys, polymer dielectrics and adhesives, ceramic dielectrics. Such complex components can be termed system-in-package (SiP). At the next higher packaging level, the SIP substrate can be soldered with larger area-array solder joints to surface mount printed wiring assemblies (PWAs) that may also contain other technologies, such as electromechanical components, (transformers, relays, switches), multi-layer circuitry, through-thickness via interconnects.

The Center for Advanced Life Cycle Engineering (CALCE) at the University of Maryland has been a premier research organization in this subject-matter for the past 35 years, partnering with industry and government partners around the world, on physics-based studies and on physics-informed AI-based studies of degradation mechanisms in advanced electronic systems, to enable more dependable (robust, reliable, safe, and secure) technologies. CALCE research includes:

- predictive multi-physics modeling to enable ***co-design*** for dependability (c-DfD),

Abhijit Dasgupta
Professor Abhijit Dasgupta conducts his research on the mechanics of engineered, heterogeneous, active materials, with special emphasis on the micromechanics of constitutive and damage behavior. He applies his expertise to several multifunctional material systems. His research contributions include solution techniques for coupled boundary value problems in multifunctional particulate and laminated composites, micromechanics approaches for constitutive properties of advanced 3-D composites, dynamic behavior and failure of thick composites, micromechanics of fatigue damage in viscoplastic eutectic-alloy composites and in short-fiber polymeric composites, and self-health monitoring in "smart" systems. Abhijit has published over 150 journal articles and conference papers on these topics, presented over 20 short workshops nationally and internationally, served on the editorial boards of three different international journals, organized national and international conferences, received six awards for his contributions in materials engineering research.

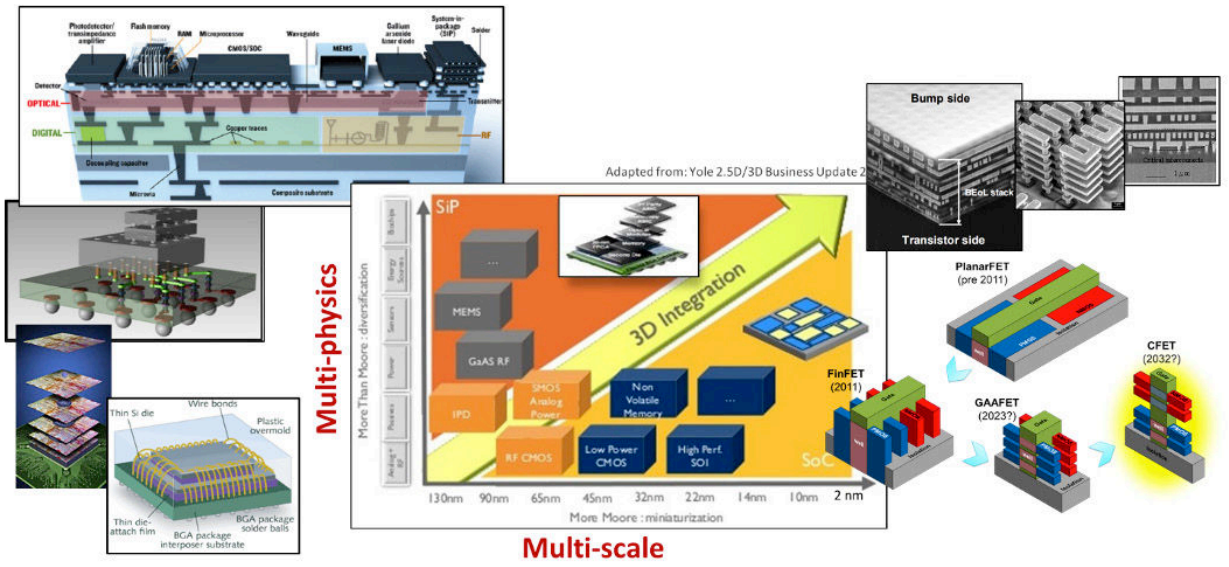


Figure 1a: Schematic of multi-physics and multi-scale HI architecture concepts (SysMoore) (adapted from Yole Corp 2015 chart)

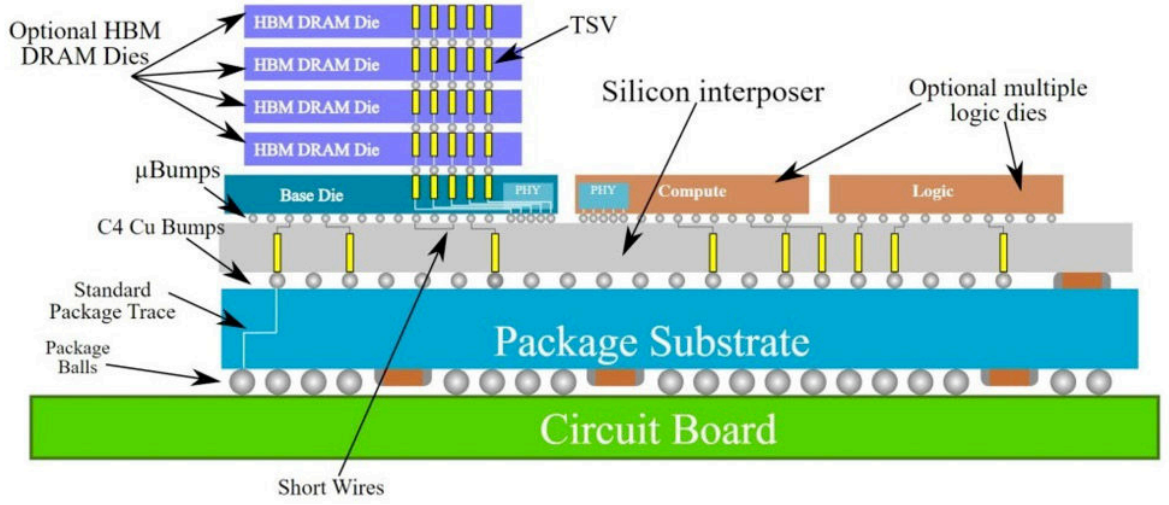


Figure 1b: Typical 2.5D/3D HI assembly [eps.ieee.org/images/files/HIR_2020/ch02_hpc_1.pdf, Source TSMC]

- ***process*** optimization, not just for yield but also for long-term dependability (PfD)
- model-assisted quantitative accelerated stress testing to enable ***qualification*** for dependability (QfD)
- model-based and data-based prognostics and continuous real-time health management throughout the life-cycle to enable ***sustainment*** for dependability (SfD)
- ***managing*** a trustable supply chain through the life-cycle, for dependability (MfD)

In particular, CALCE has conducted extensive research in temperature-driven degradation mechanisms in electronic systems. To appreciate the full scope of the influence that temperature can have on such a complex system, it is instructive to first list out the various multi-physics degradation and damage mechanisms that electronic systems can experience (e.g. excessive mechanical forces or deformations, excessive temperature or temperature cycles, excessive electrical potential gradient or current density, excessive concentration of harsh chemical contaminants and moisture, etc.).

Figure 2 shows a sample list (expressed as a chart, for convenience). The multiphysics degradation/failure mechanisms are broadly grouped as 'overstress' and 'wearout' mechanisms. Overstress mechanisms are damage mechanisms that can occur from a sudden exposure to extreme levels of any of the multiphysics loading types listed above that takes the system (and the materials it's comprised of) beyond its performance limits. In contrast, wearout mechanisms refer to gradual progressive accumulation of incremental damage associated with sustained exposure to moderate levels of the multiphysics loading types listed earlier.

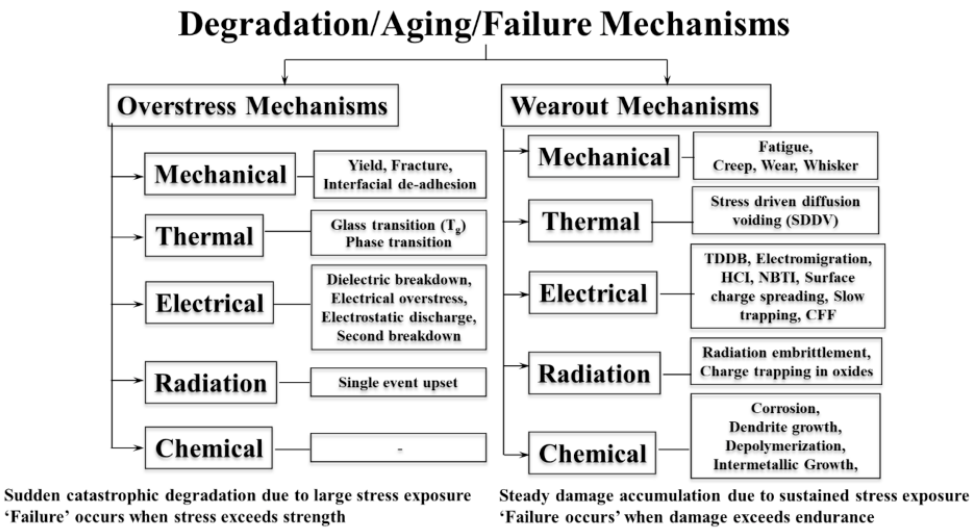


Figure 2: Multiphysics damage/aging/failure mechanisms in electronic systems (those driven by thermal and thermo-mechanical effects are discussed in more detail below)

Figure 2 provides a convenient framework to discuss the many multiphysics effects that temperature can have on the performance of electronic systems over their lifetime:

Effects of Temperature on Mechanical Degradation Mechanisms: Temperature is known to reduce the stiffness, strength and creep resistance of many materials (mostly polymers and metals) and interfaces. Since electronics use many different polymer-based dielectrics and attachment materials, as well as low-melting conductors (such as solders), excessive temperature can reduce their strength and creep resistance, thus exposing them to the risk of sudden fracture or delamination or gradual creep rupture/cavitation while under thermal and/or mechanical stresses. Creep cavitation is known to lead to problems such as stress-driven diffusive voiding (SDDV) in electronic interconnects The mechanical stresses can be a result of temperature changes (either heating or cooling) combined with thermal expansion mismatches between dissimilar materials used in electronics. These stresses can:

(i) cause warpage and complex deformation of chips, packages and distortion of photonic waveguides
(ii) affect electronic bandgap energy and dislocation mobility of semiconductor devices
(iii) generate cracking/delamination at interfaces or in bulk packaging materials (especially overstress cracking in brittle materials, e.g. in semiconductor die materials, in Extremely Low K (ELK) BEOL structures, or in ceramic dielectrics used in resistors and capacitors, or in glass substrates used in advanced packages, or in intermetallic layers seen in bonded metallic structures such as in soldered interconnects, die attach layers, wire-bonds, etc.)
(iv) cause fatigue failures in ductile materials if the temperature excursions are cyclically repeated (due to power cycling or cyclic environmental conditions).

While overstress cracking is mostly seen in brittle materials/interfaces, fatigue cracking can occur even in ductile materials/interfaces. Harsh cyclic temperature excursions, due to operational power cycling and environmental temperature swings, generate thermo-mechanical stresses at chip-package-PWB interfaces (such as thermal expansion mismatch between the die and substrate/interposer, package and the PWB, via and the PWB). CALCE has studied fatigue damage due to these cyclic thermo-mechanical stresses at packaging interfaces (such as die interfaces with the package molding compound, underfill, TIM or with surrounding substrate/interposer materials in the case of embedded dies) and in interconnection features (such as die-attach, RDLs in the package/substrate/interposer, ELK layers in the BEOL structures of the die, vias, wirebonds, solder interconnects and conductive adhesives). Examples of such failure modes in the literature are seen in *Figure 3*.

In extreme temperature spikes, materials may even experience phase transitions, e.g. polymers may cross glass transition temperatures or softening temperature, polarized ceramics can experience de-poling, etc. Temperature can also exacerbate the problem of fretting wear in separable connectors, caused by thermomechanical/vibration micromotion. Temperature can also increase the risk of whisker growth on metallic surfaces (such as tin-plated surfaces) by increasing the thermo-mechanical stresses that can assist in whisker formation and growth. [See for example Table 3 of Chapter 24 (Reliability) in Heterogeneous Integration Roadmap, eps.ieee.org/images/files/HIR_2021/ch24_rel.pdf].

Effects of Temperature on Electrical Degradation Mechanisms: Since electrical power dissipation causes temperature increases, due to self-heating effects (SHE), harsh temperatures can arise from both environmental and operational conditions. This combined temperature can cause electrical failures if there is a sudden runaway electrical condition, such as electrical overstress (EOS)

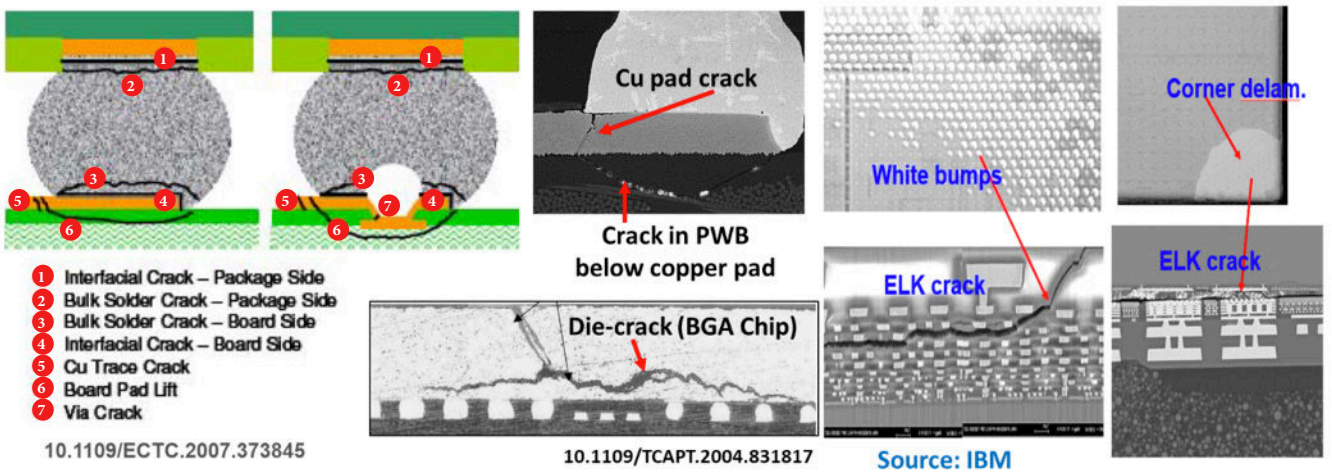


Figure 3: Failure mechanisms in interconnect systems

in conductors due to extreme current density. Sudden temperature spikes can also increase the risk of breakdown in dielectrics and oxide layer in transistors under extreme potential gradients. Sustained exposure to high temperature can accelerate a whole host of electrical degradation mechanisms such as: hot carrier injection (HCI), Bias temperature instability (NBTI/PBTI) in transistor devices; time-dependent dielectric breakdown (TDDB) in device oxide layers, slow charge trapping and contact spiking in conductor and semiconductor structures, electromigration and thermo-migration in metallic structures within the device or in the BEOL and RDL conductor layers or in external conductors and interconnects in substrates and interposers; loss of surface insulation resistance (SIR) due to electrochemical migration mechanisms such as conductive anodic filament growth (CAF) and cathodic dendritic growth.

Effect of Temperature on Chemical Degradation Mechanisms: Temperature increases the energy state and mobility of defects in materials and is therefore a well-known accelerator of diffusion and other defect migration mechanisms and chemical reactions. As a result, temperature increases the risk of corrosion of metallic conductor features in the presence of harsh ionic contaminants (either from the environment or residual impurities leftover from process chemicals), growth of brittle fragile intermetallic compounds at interfaces of bonded metallic structures (with concurrent risk of Kirkendall voiding in metal joints, e.g. at interface of solder joint and copper pad), and aging in polymers due to de-polymerization and side-chain reactions.

Temperature has a relatively low effect on degradation mechanisms due to radiation of high-energy particles, so these degradation mechanisms and modes are not discussed here.

This discussion has highlighted the complex and inter-dependent set of reliability risks that temperature can pose in complex electronic/photonic systems throughout their life cycle. Cooling solutions face increasing challenges due to ever increasing package complexity, miniaturization, and power density. However, temperature definitely has to be managed judiciously for all the reasons mentioned in this paper. Our ability to keep pace with system-level Moore's law (SysMoore) depends on academic and industry research groups working effectively together on the dual challenges of developing more effective cooling solutions and also on developing more temperature-resistant material systems for electronics applications. When designing cooling solutions, researchers and engineers need to keep in mind that the goal is not just lowering the peak temperatures, but also co-optimizing the severity of temperature cycles, temperature gradients and temperature transients.

The role of temperature in any one degradation mechanism can be quite complex. As an example, consider a study of solder joint fatigue in flip-chip assemblies due to accelerated temperature cycling tests during design verification testing (DVT) [https://doi.org/10.1115/1.2793846]. Flip chip dies are routinely mounted on organic substrates/interposers, causing a large CTE mismatch (2.5-3.5 ppm/°C for Si vs 15-20 ppm/°C for in-plane expansion of typical fabric-reinforced organic substrate materials) [*Figure 4*]. Consequently, the corner solder joint in a 10mm x 10 mm flip-chip component can experience as much as 4% shear strain for every 10 °C change in temperature, resulting in fatigue failures in a few hundred temperature cycles in accelerated stress testing. A common solution therefore is to add an underfill, which is typically a filled polymer that is carefully tailored to the flip chip assembly for the appropriate mechanical, thermomechanical, electrical and moisture absorption characteristics. Underfills can improve fatigue durability by 1-2 orders of magnitude, but the addition of these new materials and processes further complicates the assembly process.

When it comes to fatigue damage, a decrease in temperature can be as damaging as an increase in temperature. In the case of sol-

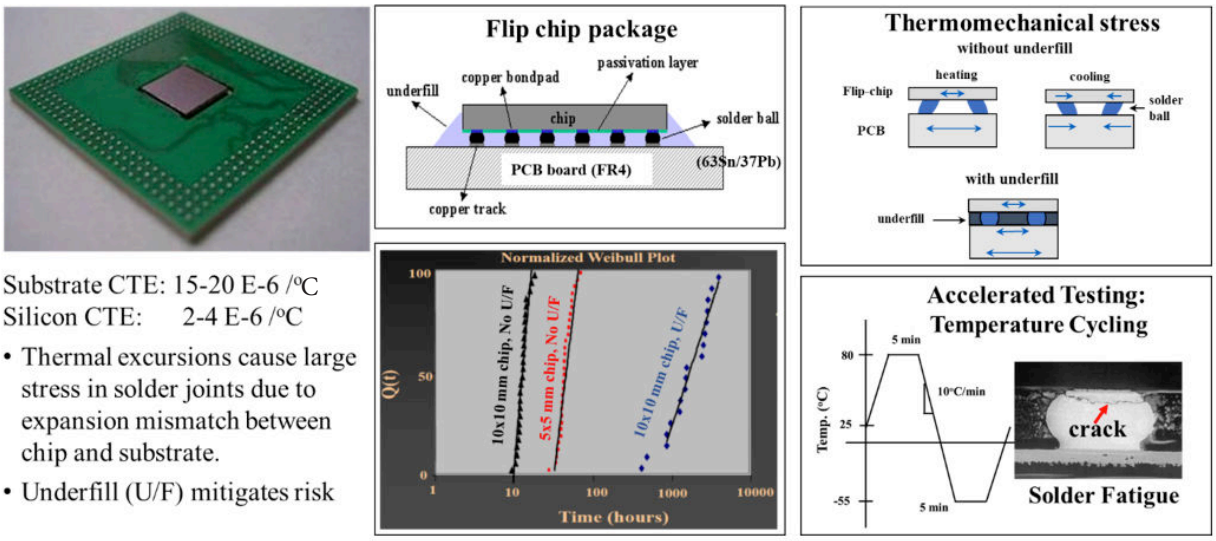


Figure 4: Thermal cycling fatigue in Flip-Chip Solder Joints

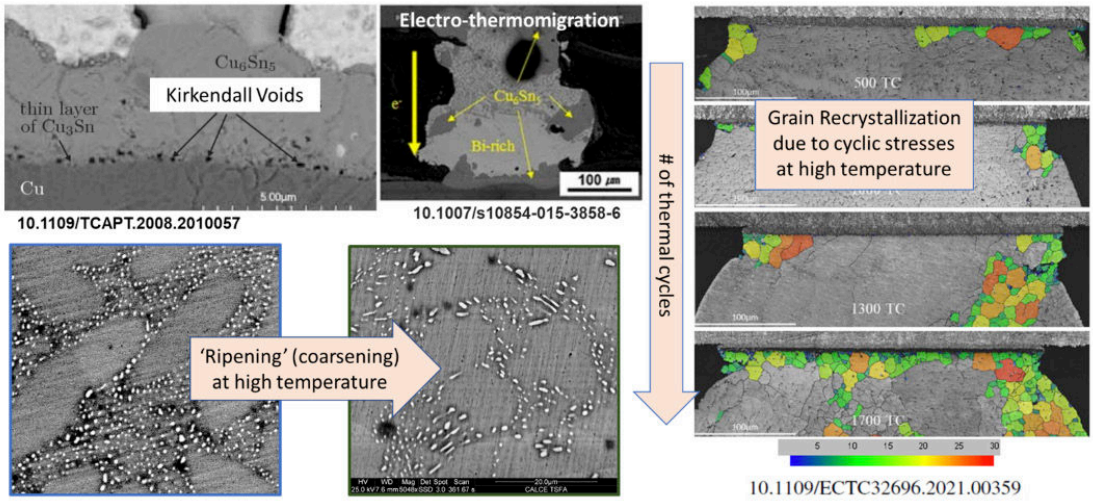


Figure5: Additional thermally activated degradation mechanisms in solder interconnect systems

der however, increasing temperature not only causes thermal expansion mismatch but also reduces creep resistance of the solder, thus increasing the strain severity in the solder. High temperature causes several additional degradation modes (*Figure 5*), such as:

(i) aging of solder microstructure ('ripening'), further decreasing the creep resistance of the solder material
(ii) growth of intermetallic layers at the solder pads (with concurrent risk of Kirkendall voiding in the pad), further embrittling the connection between the solder and the UBM/pad
(iii) electromigration and thermo-migration in the solder joint, further weakening the joint
(iv) recrystallization of solder grains due to temperature cycling, further decreasing the creep resistance and increasing the risk of intergranular fatigue fractures.

Managing these multiple risks requires the right combination of solder alloy material, under-bump metallization (UBM) system and plating system on the substrate pad.

In contrast, a corresponding drop in temperature causes the same expansion mismatch, but increases the solder's creep resistance, thus reducing the amount of shear deformation in the solder joint. However, an increase in creep resistance of the solder may also produce competing negative effects on the rest of the assembly, due to corresponding increase in the stresses in copper pads/traces, RDLs, ELK structures, and microvias.

Continued research focuses on balancing these competing risks through careful and precise system-level optimization, thus making DfR (design for reliability) a very important part of system co-design.

Design Considerations for Chip/Package Level Bare Die Impingement Cooling for High Performance Computation Systems

Tiwei Wei
Purdue University

With the rising demand for more powerful, efficient, high-performance computation (HPC) systems, power densities of devices have increased dramatically. To cope with the increasing heat flux challenge for future data center servers beyond 1 kW/cm^2, efficient liquid cooling solutions are needed to address those thermal challenges. In the landscape of advanced electronic cooling solutions, various options exist, ranging from embedded microchannel cooling to inter-die layer cooling, encompassing single-phase to two-phase jet cooling. However, from an industry perspective, challenges associated with direct embedded microchannel cooling, such as escalating costs and reliability issues, currently remain substantial barriers to their implementation in high-power and high-performance chips within data centers. The expensive and high-risk nature of the etching process on the processor backside further complicates matters for chip manufacturers [1]. The bare-die impingement jet cooling solution shown in *Figure 1(a)* presents a compelling alternative that circumvents the need for postprocessing of the processor backside. In bare die cooling, liquid coolant is directly ejected from jet nozzles on the chip backside, resulting in exceptional thermal and hydraulic performance, lower thermal resistance, and reduced pumping power

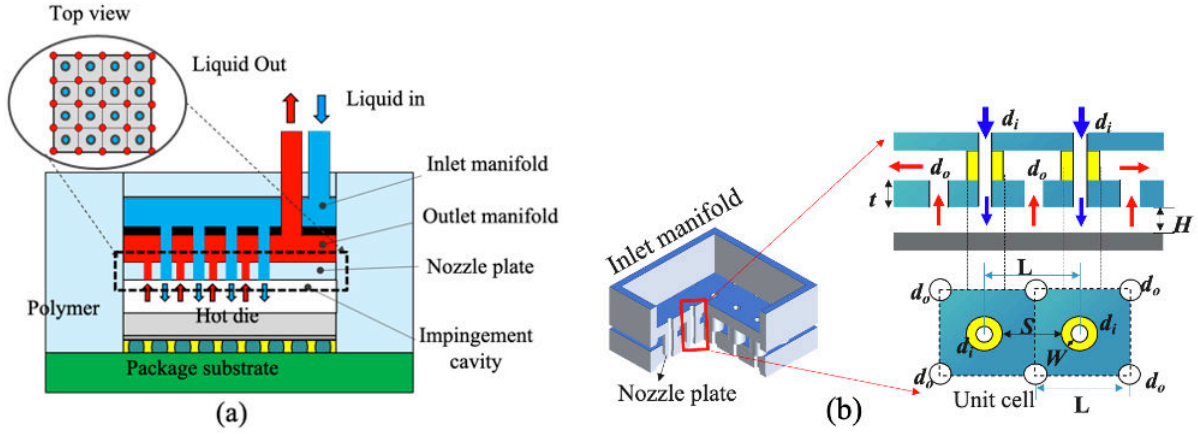


Figure 1: Chip level bare die cooling solutions for high performance system: (a) schematic of the bare die cooling concept; (b) geometry critical dimensions for parameter investigations [2]

Tiwei Wei
Dr. Tiwei Wei, Assistant Professor at Purdue University's School of Mechanical Engineering, boasts a diverse academic background. He completed a postdoctoral research tenure at Stanford University's NanoHeat lab (2020-2022) and earned his Ph.D. from imec and KU Leuven, Belgium (2020). Prior, he held senior research positions at Tsinghua University and Hong Kong University of Science and Technology (2011-2015). Specializing in semiconductor packaging and thermal management, Dr. Wei has authored 60+ publications, 10+ patents, and actively engages in academic contributions, chairing sessions, and leading roles in IEEE Electronic Packaging Society (EPS) Silicon Valley Chapter and Central Indiana Chapter.

consumption [2]. These attributes make it highly promising for near-term implementation within industry data center systems. Therefore, system design guidelines are needed to design an energy efficient bare die jet cooling, including the nozzle parameters, manifold optimizations as well as material reliability.

In this article, parametric analysis of an impingement cooling geometry is introduced. After that, an innovative manifold design is investigated and compared. Lastly, the packaging processes and material-compatible bare-die jet cooling solutions will be discussed. *Figure 1(b)* shows a graphical representation of the geometrical parameters of the unit cell for an impinging system with an N×N array of inlet nozzles and distributed inlets with inlet diameter d_i, outlet diameter d_o, cavity height H, nozzle plate thickness t, chip thickness t_c and unit cell size L. The unit cell size is defined as the ratio between the chip size S_d and the nozzle row number N: $L = S_d / N$. The chip area in this study is fixed at 8×8 cm^2.

Design Guidelines for On Cooler Nozzle Parameters

In this study, we investigated different design variables to identify their best combination, focusing on thermal resistance and pumping power independently. A specific cooler's thermal behavior, with fixed dimensions, was analyzed across various pressure drops and flow rates, represented in *Figure 2(a)* and *2(b)*. The thermal resistance scales inversely proportional with the chip size (resulting in lower thermal resistance values for large chips), while the pumping power scales proportionally with the area (resulting in high required pumping power for large chips). To compare the intrinsic cooling performance of the different coolers, all quantities are normalized with respect to the chip area, A. Therefore, the normalized thermal resistance $R_{th}^* = R_{th}^* A$, and the normalized pumping power $W_p^* = W_p/A$. Different cooler geometries can be compared on these charts, and the curve closest to the origin represents the Pareto front for optimal thermal solutions. Based on the characteristic curves, the designer can choose the optimal value based on a constrained flow rate or pressure drop. In this study, we used water as the liquid coolant.

Figure 2 indicates a key trend: thermal resistance saturation with increasing nozzle density (N) under constant cavity height. In *Figure 2(a)*, characteristic curves depict the trade-off between thermal resistance (R_{th}^*) and pumping power (W_p^*) for various cooler arrays and flow rates (50 mL/min to 530 mL/min). The analysis maintains a constant nozzle diameter ratio (d_i/L), ensuring a consistent nozzle area when altering N. The design range for d_i/L is from 0.01 to 0.4. Since the Reynolds number ranged from 32 to 2024, a laminar model and transition SST model were used in this study. With a constant flow rate, R_{th}^* decreases as flow rate rises for a fixed N, but pumping power concurrently increases. Notably, an asymptotic behavior emerges for higher N, and the pumping power initially decreases but then grows again as N increases. A similar trend is observed in *Figure 2(b)* under a constant pressure drop.

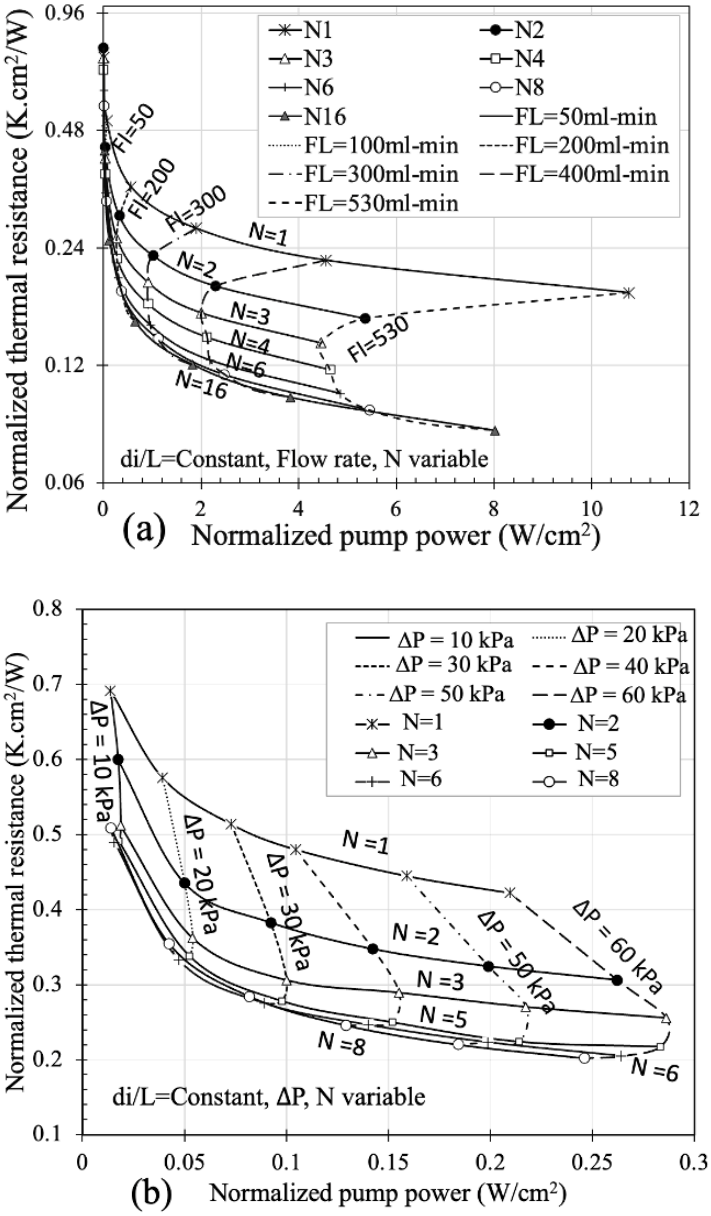
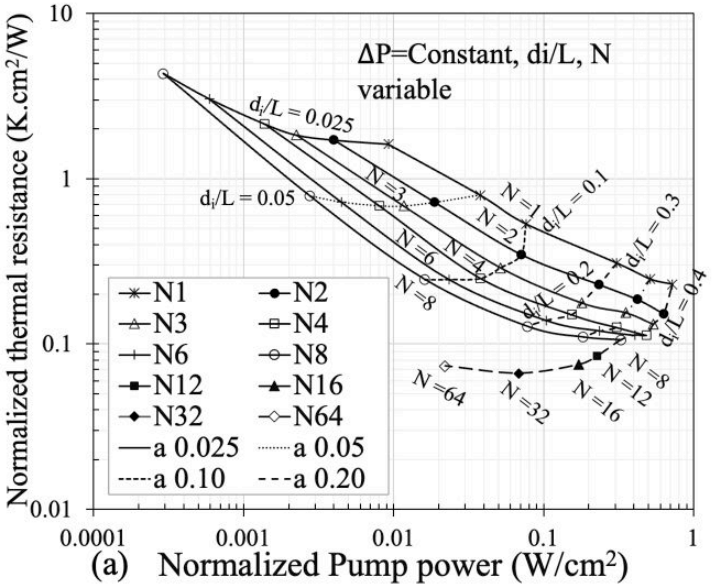


Figure 2: Characteristic curve of the cooler with different nozzle number and (a) flow rate and (b) pressure drop, with d_i/L kept constant (d_i/L=0.1, H=0.2 mm)

The following steps explore the impact of nozzle diameter in a trade-off chart with constant pressure drop and constant flow rate constraints. The nozzle diameter ratio (d_i/L) varied from 0.025 to 0.4, with nozzle number (N) ranging from 1 to 64. In *Figure 3(a)*, with constant N and pressure drop (ΔP), thermal resistance decreases as nozzle diameter increases, leading to an increase in pumping power due to higher inlet velocity to meet the fixed pressure drop constraint. Conversely, for a constant nozzle diameter, thermal resistance decreases initially and then increases with rising N, while pumping power decreases with increasing N. *Figure 3(b)* presents a similar trade-off chart for a constant flow rate, showing different trends compared to a constant pressure drop. For constant N, thermal resistance reduces

as d_i/L decreases, while pumping power increases due to higher inlet velocity. With constant d_i/L, both thermal resistance and pumping power decrease initially and then increase with increasing N.



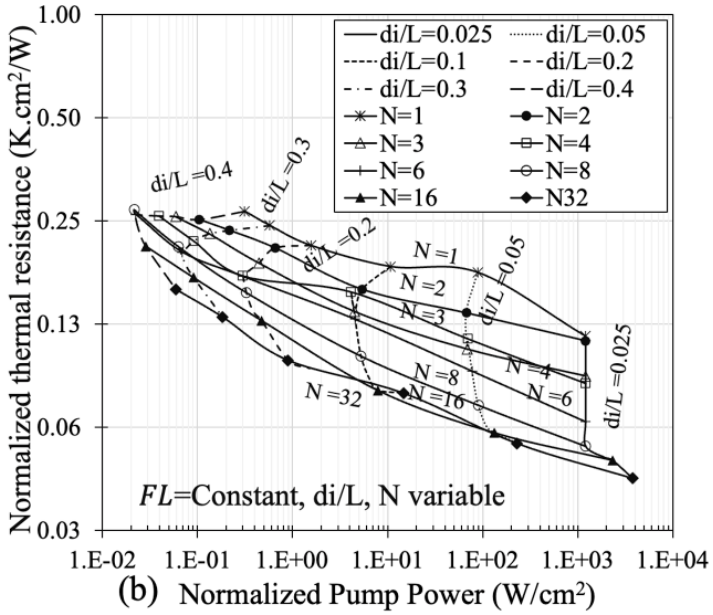


Figure 3: The characteristic curve with different nozzle diameter ratio and inlet number N under (a) constant pressure drop=40 kPa; (b) constant flow rate=530 mL/min, at H=0.2 mm). (Note: a in *Fig 3a* represents d_i/L)

In summary, optimizing the nozzle diameter and number in a jet cooling system has significant effects on thermal performance and pumping power. Varying these parameters allows designers to find a balance, considering factors such as thermal resistance and pumping power, ultimately influencing the efficiency and effectiveness of the cooling system.

Advanced Manifold Level Design Methodology

In a previous study, the importance of the manifold level optimization is discussed [3]. It is shown that the manifold level design of this microfluidic cooler is very important for the overall cooler performance, since it determines the flow uniformity and system level pressure, especially for large area die size applications. Our results indicate that the pressure drop analysis of a 3D printed full cooler level shows that the manifold level is responsible for the majority (80%) of cooler pressure drop, including the inlet and outlet manifold. Furthermore, the inlet manifold defines the coolant flow distribution over the chip [3]. The flow uniformity can further determine the temperature gradient across the chip surface, which is important to improve the design. In this section, three innovative designs are proposed and compared to the initial standard design. These include a mushroom manifold design, isolated jet nozzles and finger-shape manifold design. The thermal and hydraulic performance analyses are based on CFD modeling results.

Mushroom Manifold Design

As illustrated in the flow distributions of the multi-jet impingement cooling in *Figure 4*, the inlet flow goes into the inlet chamber, showing a mushroom shape. However, the flow at the top corner of the manifold introduces significant pressure losses. Therefore, a mushroom shape inlet manifold is proposed to reduce the pressure drop. The CAD design structure is shown in *Figure 4* with an internal visualization and the cross-section view of the cooler.

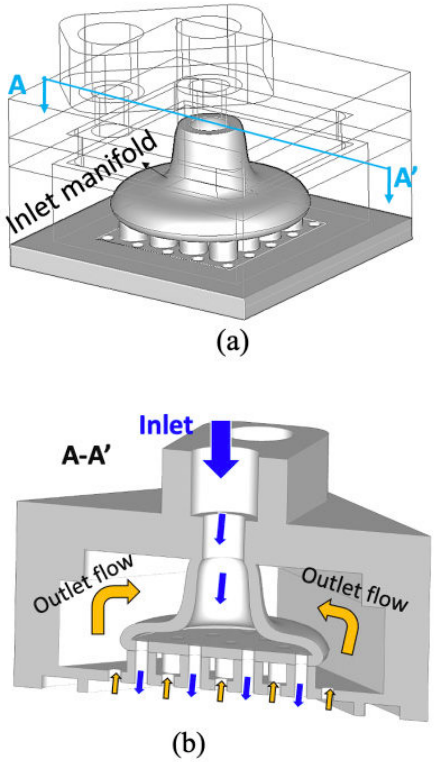


Figure 4: Mushroom manifold design: (a) internal visualization of the mushroom inlet manifold design; (b) cross section view of the new design with indication of the flow directions

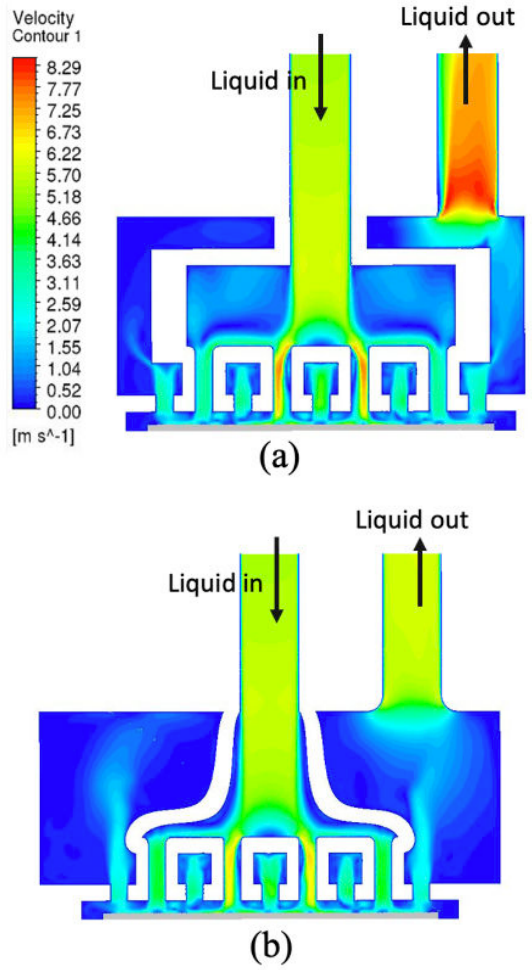


Figure 5: Velocity distribution comparison for the (a) standard cooler design and (b) mushroom design (chip power=50W, flow rate=1 L/min)

For the comparison of the mushroom design and standard design, CFD modeling was used to evaluate the chip temperature and pressure drop. The flow rate used in this comparison is 1 L/min. The chip power of 50 W was applied to the 8×8 mm^2 chip. The flow distributions for the two designs are shown in *Figure 5*. It can be seen that much more design volume space is transferred to the outlet manifold. Moreover, the velocity distribution across the inlet nozzles shows better flow uniformity. The modeling showed that the mushroom design reduced the pressure drop by 40%, and the average chip temperature by 10% for the same temperature gradient, as shown in *Table 1*.

Design	Standard design	Mushroom design
Pressure drop (kPa)	45.1	305
Averaged chip temperature (°C)	24.9	21.9
Temperature gradient (°C)	3.4	3.1

Table 1: Performance comparison between the standard design and mushroom design

Isolated Nozzles Design

The standard design shown in *Figure 6* has locally distributed outlets that provide very short paths to the outlet manifold. However, this requires the outlet flow to pass through outlet nozzles that add significant pressure drop. To eliminate this extra pressure drop, isolated inlet nozzles were evaluated; as shown in *Figure 6(b)*, the outlet nozzles were replaced by an open area inside the manifold.

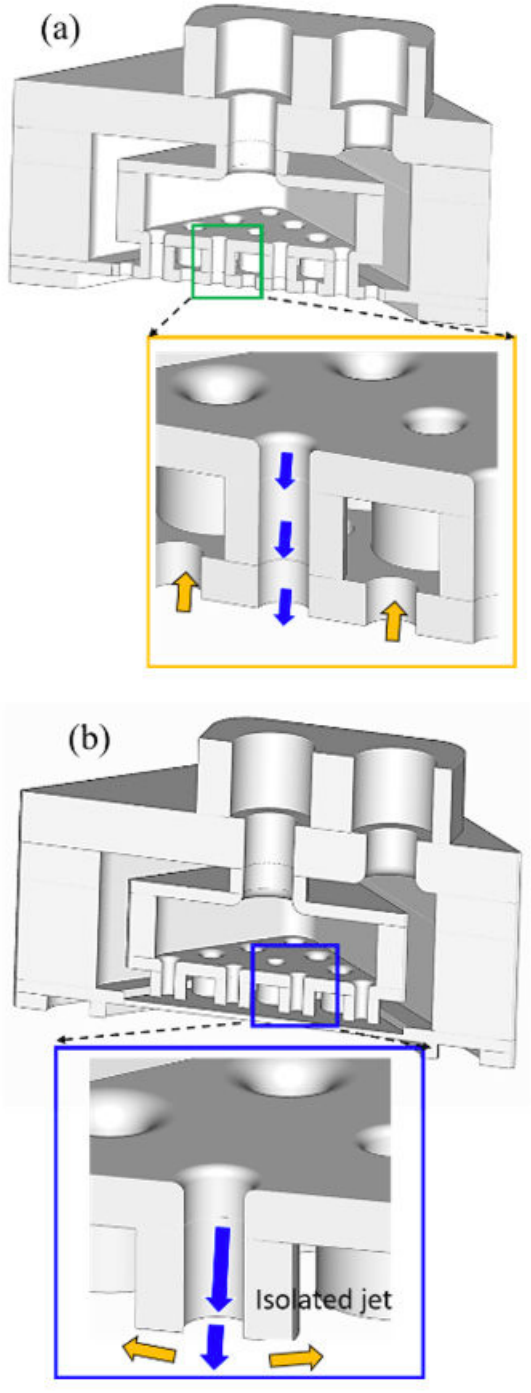


Figure 6: (a) Initial standard design with locally distributed outlets; (b) Isolated jet for outlet manifold level design

The temperature and pressure drop comparison between the initial vertical feeding design and isolated jet design are compared systematically in *Table 2*. In general, the isolated jet cooling shows worse thermal performance than the initial design with locally distributed outlets. The initial outlet nozzle plate confines the wall jet region on the cooling surface, resulting a lower temperature. The open area outlet flow for isolated jet cooling can lead to cross flow effects inside the cavity, which can influence the temperature gradient of the chip, shown in *Figure 7*.

Design	Standard design	Isolated jet
Pressure drop (kPa)	45.1	42.6
Averaged chip temperature (°C)	24.9	26.5
Temperature gradient (°C)	3.4	9.9

Table 2: Performance comparison between the initial design and mushroom design

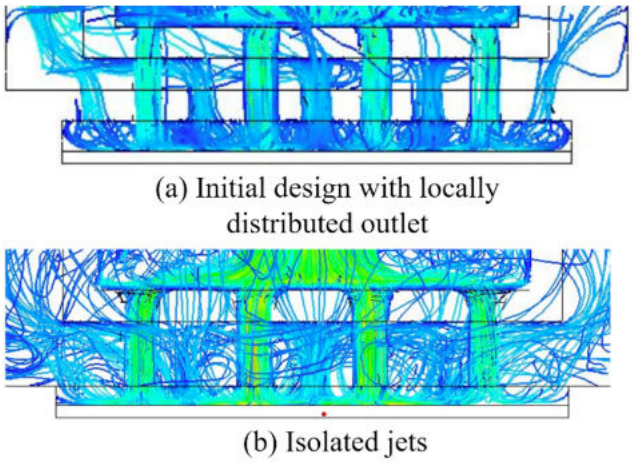


Figure 7: (a) Initial standard design with locally distributed outlets; (b) Isolated jet for outlet manifold level design

Finger-shape Manifold Design

Lateral feeding designs show significant advantages relative to vertical feeding designs. However, this design still needs two layers: one for the inlet manifold and the other for the outlet manifold. This conflicts with the need for thinner coolers to be compatible with chip packaging design requirements. Therefore, a finger shape design that combines the inlet manifold and outlet manifold into one manifold layer is proposed (*Figure 8*). This allows the cooler thickness to be reduced by a factor of 2.8, relative to a conventional lateral feeding design with two layers. The inlet manifold and outlet manifold are separated by the solid wall. A full scale CFD model is also performed for the finger-shape design. The CFD model and meshed model with the fluid domain are extracted from the CAD structure. The flow rate is 1 L/min, under chip power of 50 W.

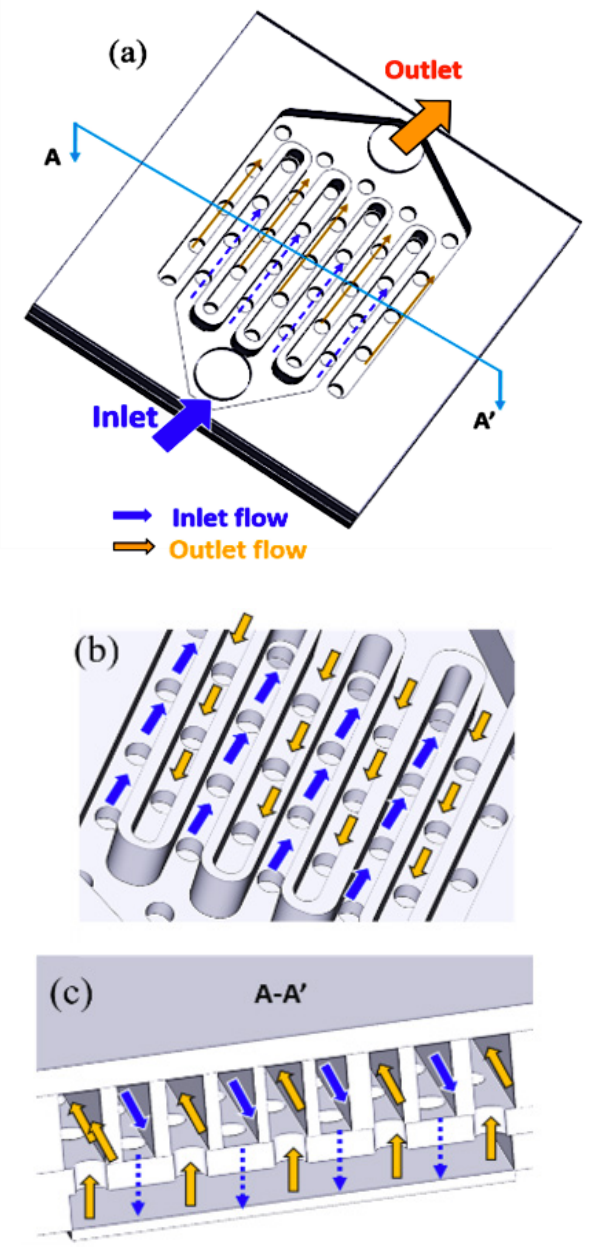


Figure 8: Schematic of the finger-shape manifold design:(a) entire CAD design structure; (b) snake shape design with local channels

Design	Standard design	Thin manifold design	Snake shape design
Pressure drop (kPa)	45.1	163	65.0
Averaged chip temperature (°C)	24.9	24.7	23.2
Temperature gradient (°C)	3.4	8.1	5.8

Table 3: Performance comparison between the initial design and mushroom design: use the previous design

The temperature comparison shows that the thin manifold design with vertical feeding results in a lower temperature in the chip center while the hottest temperature is around the chip corner. For the finger-shape design, the lowest temperature is at the end of the inlet manifold, where we expected recirculation at those locations. The highest chip temperature is at the end of the outlet manifold, showing less flow rate at those locations. In addition, the thermal and hydraulic performance are compared, including the averaged chip temperature, pressure drop and temperature gradient. The finger-shape design shows a 40% thinner cooler (from 5 mm to 3 mm) and the pressure drop reduced by a factor of 2.5. Moreover, the temperature gradient can be improved by a factor of 1.4, as shown in *Table 3*. In general, the finger-shape manifold design shows great advantages of the cooler thickness and the pressure drop reduction.

Cooler Materials for Reliability Exploration

The bare die jet cooler assembly process offers two cooler assembly options: the first is to assemble the package to the board and then attach the cooler to the package with adhesive or clamping. An advantage of this assembly approach is that it does not introduce a high temperature requirement for cooler material. In the second assembly option, the cooler is first mounted and sealed on the package before the package and cooler are assembled to the PCB. This assembly option introduces the need to survive the reflow temperature (250°C). The exploration of various cooler materials for enhanced reliability encompasses a diverse range of options, such as materials with low CTE and/or, high Heat Deflection Temperature (HDT) and new manufacturing methods. One method involves additive manufacturing techniques with CTE- modified polymer-based materials that can provide flexibility and adaptability in cooler design [4].

In addition, glass-based coolers can offer unique thermal properties and durability [5]. Metal 3D-printed direct liquid jet-impingement cooling stands out as an innovative solution, leveraging advanced manufacturing methods for efficient and precise thermal management [6]. Additionally, ceramic-based coolers contribute to the reliability landscape, bringing high-temperature resistance and mechanical strength [7]. Each of these materials presents distinct advantages, and their exploration underscores the ongoing quest for cooler materials that meet the demanding requirements of reliability in various applications.

Conclusion

This article highlights the potential of bare-die impingement jet cooling for high-performance computing systems. It explores nozzle parameter optimization, advanced manifold design, and various materials for enhanced reliability. The findings demonstrate the importance of achieving a trade-off between the thermal resistance and pumping power while offering innovative manifold design solutions to improve overall cooler performance. The study offers insights and guidelines for thermal engineers in designing efficient and reliable cooling systems for high-performance data centers.

References

[1] Wei, Tiwei. "All-in-one design integrates microfluidic cooling into electronic chips." (2020): 188-189.

[2] Tiwei, T., Oprins, H., Cherman, V., Van der Plas, G., De Wolf, I., Beyne, E., & Baelmans, M. (2017, December). High efficiency direct liquid jet impingement cooling of high-power devices using a 3D-shaped polymer cooler. In 2017 IEEE International Electron Devices Meeting (IEDM) (pp. 32-5). IEEE.

[3] Wei, T. W., H. Oprins, V. Cherman, E. Beyne, and M. Baelmans. "Experimental and numerical investigation of direct liquid jet impinging cooling using 3D printed manifolds on lidded and lidless packages for 2.5 D integrated systems." Applied Thermal Engineering 164 (2020): 114535.

[4] Fei, Guanghai, Tiwei Wei, Qimin Shi, Yongjian Guo, Herman Oprins, and Shoufeng Yang. "Preliminary study on hybrid manufacturing of the electronic-mechanical integrated systems (EMIS) via the LCD stereolithography technology." (2019).

[5] Wei, T. Ph.D. thesis (2023). "High Efficiency Polymer based Direct Multi-jet Impingement Cooling Solution for High Power Devices." arXiv preprint arXiv:2310.11663.

[6] Pappaterra, Antonio, et al. "Advanced (Metal 3D-Printed) Direct Liquid Jet-Impingement Cooling Solution for Autonomous Driving High-Performance Vehicle Computer (HPVC)." EuroSimE. IEEE, 2021

[7] Lin, Yujui, Tiwei Wei, Wyatt Jason Moy, Hao Chen, Man Prakash Gupta, Michael Degner, Mehdi Asheghi, H. Alan Mantooth, and Kenneth E. Goodson. "Multi-level embedded three-dimensional manifold microchannel heat sink of aluminum nitride direct bonded copper for the high-power electronic module." Journal of Electronic Packaging 146, no. 1 (2024): 011006.

Thermal Analysis Methodology Best Practices

Adolfo Lozano III, PhD, PE
Senior Principal Mechanical Engineer, Collins Aerospace, an RTX Business

Introduction

Thermal analysis: It's a field that every mechanical engineer is exposed to during their undergraduate studies and many practice at some point during their professional careers. It's also a field that some devote their full-time careers to as dedicated thermal engineers (or thermal analysts). Regardless of where in the broad spectrum of mechanical engineering work scope you may fall, whether you typically perform a single brief thermal analysis per year or practice it daily, you may find this manuscript regarding thermal analysis methodology valuable and edifying. The objective of this manuscript is to clearly and systematically outline best practices with regard to thermal analysis methodology that enable an accurate, well-executed analysis. In the context of this manuscript, the primary focus is on electronics systems for ground-based and airborne applications in the aerospace/defense industry.

First, it is important to define what thermal analysis is. Thermal analysis broadly encompasses the task of solving the temperature and flow fields of an electronics system in a given application and environment; it solves the conjugate heat transfer problem, which couples the conservation of energy, conservation of mass, and conservation of momentum equations. The conservation of momentum equations are more famously known by mechanical engineers as the Navier-Stokes equations from their undergraduate fluid dynamics courses. In fact, the Navier-Stokes equations are, in essence, the conservation of linear momentum equations with the constitutive equation for a fluid continuum substituted in for the Cauchy stress tensor term. Standard computational fluid dynamics (CFD) software has the capability of solving the conjugate thermal-flow problem. Among the biggest players in the industry are Fluent (ANSYS) and STAR-CCM+ (Simcenter).

Next, it's important to define what thermal analysis is not. Thermal analysis is not pushing a button, running a solution, getting a pretty picture of temperature or flow contours, and reporting the results. To their detriment, many computer-aided design (CAD) engineering software, which are used primarily by the mechanical engineer (ME) with the 'ME designer' role rather than the 'thermal engineer' role, now offer a one-stop shop for mechanical design and thermal simulation. Mechanical designers are able to quickly get a thermal solution without necessarily having the experiential or analytical background to verify the accuracy of the solution. Rather, thermal analysis entails understanding and ensuring that the boundary conditions, thermophysical material properties, and modeling assumptions used are reasonably accurate. It entails reviewing modeling results with a healthy degree of suspicion (i.e., "guilty until proven otherwise" philosophy), sanity-checking them with simplified hand calculations, and convincing yourself that the simulation is indeed accurate. It entails using the analysis as a tool to guide the mechanical design of a system from a concept to a feasible design.

Now that we've outlined a broad definition of thermal analysis, let's explore critical methodology steps in the thermal analysis process. Following each of these steps will help to ensure an accurate analysis.

Adolfo Lozano III, PhD, PE
Adolfo is a Senior Principal Mechanical Engineer at Collins Aerospace, an RTX Business. He joined RTX in 2011. His 13 years of work experience include 11 years in thermal design & analysis, 1 year in engineering operations, and 1 year in program management as an Integrated Product Team Lead (IPTL) & Control Account Manager (CAM). He holds degrees in mechanical engineering (BS 2008, MS 2011, PhD 2020) and is a licensed Professional Engineer (PE) in Texas. He has 8 RTX symposium presentations (2013-2022), 2 Collins Aerospace Electronics Cooling Community of Practice (CoP) presentations (2023), 4 peer-reviewed publications (2011-2021), and 1 patent as co-inventor (2022).

Best Practice #1: Fundamentals

Nothing beats having a deep, thorough, and technical understanding of the relevant, underlying physics. Textbook knowledge is a requisite for analysis—here, primarily thermodynamics, fluid dynamics, and heat transfer (all modes) [1]. Because thermal/fluids phenomena may not be obvious or intuitive to all, a fundamental technical understanding can only be achieved by studying the relevant textbooks from a standard undergraduate curriculum in mechanical engineering. In fact, as I often advise undergraduate students, the most successful engineers in industry are those who have a well-developed and intuitive understanding of the relevant physics and, more importantly, are able to communicate that to their peers and leadership. Understanding the fundamentals enables the engineer to think critically when faced with challenging, complex, and non-textbook problems that are commonplace in industry. The following brief outline of fundamental topics for each mode of heat transfer will help prepare the thermal engineer in an electronics cooling framework.

From a conduction standpoint, understanding conductive resistances due to one-dimensional conduction through multi-layered materials is necessary to calculate expected temperature rises or the composite material's effective thermal resistance [°C/W] or thermal conductivity [W/m/K]. Calculating fin (i.e., extended surface) parameters is useful for quantifying effective fin performance and simplifying modeling efforts. Understanding energy storage (i.e., adiabatic heating of a solid or incompressible liquid) based on a material's thermal capacitance, which is inherently a transient/diffusion problem, will help calculate the expected temperature rise or time duration $\left(\frac{\Delta T}{\Delta t} = \frac{\dot{Q}}{\rho V c}\right)$

From a convection standpoint, understanding convective resistances due to free (natural) and forced convection based on a convective heat transfer coefficient (h value) is important for estimating surface temperatures and the temperature rise through the boundary (film) layer. The lumped capacitance approach facilitates calculating transient responses of a solid in a convective environment if the Biot number can be shown to be much smaller than unity. Understanding dimensionless numbers (e.g., Re, Pr, Ra, Gr, Nu, etc.) and their relevance to certain applications will help characterize the flow regime or relevance of empirical correlations. In general, the field of convection is a patchwork of various empirical correlations for a range of geometries under specific flow conditions, owing to the non-analytical nature of solutions to the Navier-Stokes equations. Therefore, having a reference repository of the relevant correlations for internal and external flow for flat plate or finned geometries will enable accurate thermal characterization efforts [1][2][3][4]. In fact, to many non-thermal engineers' surprise, translating a fluid mass flow rate to a convective heat transfer coefficient is not necessarily a trivial exercise; it entails coupling the caloric rise in the fluid from a first law energy balance ($Q = \dot{m}c_P\,(T_{OUT} - T_{IN})$) to Newton's law of cooling ($Q = hA(T_{SURFACE} - T_{FLUID})$), which can be coupled only via an empirical, geometry-specific Nusselt ($Nu = hL/k_{FLUID}$) or Colburn ($J = St\,Pr^{0.67}$) correlation [5]. Other relevant convection fundamentals include pressure drop (head losses) of fluid flow through an orifice, duct, and fittings [6]. As a side note, Ref. [7] provides an enjoyable collection of anecdotes illustrating conductive and convective heat transfer principles.

Finally, from a radiation standpoint, radiative cooling is generally not a primary cooling mechanism for most ground-based and airborne defense applications—the exception being cases in which hardware is primarily cooled via free convection. Radiation does, however, represent a critical cooling effect in rarefied gas and space applications. Therefore, it is important to understand surface emissivity, shape factors, and the temperature dependence relationship of radiation exchange between surfaces. Radiative heating (or environmental heating), in contrast, whether from aerodynamic air friction due to high-speed convective flows (colloquially, "aeroheating") or incident solar radiation, can represent critical boundary conditions for airborne applications (and the latter for ground-based and space applications too). Aeroheating entails understanding the total air temperature of a certain flow, which is approximated by the recovery temperature (i.e., Eckert or adiabatic wall temperature). In aeroheating scenarios, a heat shield may be necessary to protect electronics from undesirable heating and may be accomplished from a low-emissivity (high reflectivity) or a low-thermal conductivity material depending on the driving mechanism of heat infiltration. In short, unless specifically dealing with solar radiation, supersonic speeds, or free convection designs, radiative cooling is typically not a primary cooling mechanism for electronics hardware in most ground-based and airborne applications.

Best Practice #2: Peer Review

As project deadlines loom or organizations grow, it's natural to circumvent and minimize the value of a critical peer review. This is particularly true for fast-paced analyses supporting projects driven by cost and schedule more than technical rigor. However, it is important to fight the urge to skip a thorough and comprehensive peer review and instead hold one at the appropriate time. The appropriate time for a peer review is late enough that (1) sufficient progress in the analysis has been made such that a peer review is a reasonable and value-added task, but (2) not so late that any major analysis errors or blind spots identified in the review cannot be corrected in time for the analysis deadline, typically a design review, customer presentation, or deliverable report. Therefore, holding desk checks (i.e., informal or mini peer reviews) early and often is a good practice.

Peer review, by definition, is intended to have a fresh pair (or pairs) of eyes review the model and analysis in detail—ideally from experienced, senior engineers who are subject matter experts (SMEs). Peer review entails a technical deep dive into the analysis, including reviewing the model simulation and all relevant aspects (boundary conditions, geometry, assumptions, material thermophysical properties, etc.). It's an unreasonable expectation for an engineer to be 100% right 100% of the time; everybody has blind spots or misses, and it's natural for some-

thing to "fall through the cracks" for even the most experienced engineers. Although difficult at times, peer reviews require a degree of humility by the analyst and ultimately make an organization stronger by ensuring that analyses have been verified to be accurate. It's difficult to overemphasize the value of peer review.

Best Practice #3: Sanity Checks

Sanity checks are a critical tool in the thermal engineer's analysis armamentarium [8][9]. Sanity checks serve to verify the accuracy of a computational simulation and can be done in piecewise or aggregate approaches. A sanity check is simply a hand calculation—whether on paper, spreadsheet, or analysis tool like Mathcad (PTC) or MATLAB (MathWorks)—with simplifying assumptions to make the problem more feasible for an analytical solution. For example, the temperature rise due to heat conduction through a material (or material stack) with a uniform heat flux assumption would not account for localized heat fluxes nor lateral heat spreading effects but would provide a minimum ΔT value expected. Similarly, the transient temperature rise due to adiabatic heating (energy storage) of a lumped continuum (fluid or solid) in a closed system would not account for any convective or radiative cooling effects but would provide a maximum ΔT value expected. Similarly, the pressure drop due to fluid flow through a fin core (fin stock) or orifice plates would neglect minor head losses due to fittings and ducting bends but would provide a minimum ΔP value expected [2][3]. If constructed correctly, a sanity check could estimate the primary driving effects reasonably well while leaving secondary effects for the computational simulation to resolve in detail.

The truth is, nearly anybody can learn how to build and solve a CFD model. But without a technical background in the relevant thermal/fluids physics that the thermal engineer has learned both academically and experientially, the risk of a "garbage in, garbage out" exercise is high. The "garbage in, garbage out" caveat simply refers to the situation where erroneous model inputs (boundary conditions, properties, or assumptions) will yield erroneous model results. The practice of sanity-checking a simulation is what sets the experienced thermal engineer apart. The key to a sanity check exercise is knowing what formulas and equations are relevant to the specific application. Performing an energy balance (conservation of energy) on a control volume ($E_{IN} - E_{OUT} = E_{STOR} - E_{GEN}$) or going straight to the heat conduction equation and simplifying ($k\nabla^2T = \rho c_p \partial T/\partial t - Q_V$) would be a good starting point. A sanity check is ideally done for every analysis performed by the thermal engineer, which also helps commit relevant formulas and equations to memory, which can be too easy to forget with daily, non-analysis tasks engineers encounter in industry.

Furthermore, a related best practice that is important and necessary in any thermal analysis is model validation with test data. Simply put, models are validated with empirical data once the analyzed hardware is available to test. To quote Prof. Richard P. Feynman, "If it disagrees with experiment, it's wrong." Test validation is especially critical for deliverable products. Many references in the literature emphasize the importance of model validation that the reader is referred to [10].

Best Practice #4: Documentation

The goals in a documentation effort, whether in report or presentation format, are primarily twofold: (1) present the results of the analysis in a clear way, and (2) outline the methodology taken such that a fellow expert in the field can reasonably recreate the analysis and results. If the analysis or experiment is documented in a way that precludes verifiability or repeatability, then the documentation effort failed to accomplish its purpose.

Ideally, a thoroughly documented thermal analysis generally encompasses the following sections:

- Executive summary, which states the bottom line up front (BLUF) in a short and concise paragraph
- System Overview
  - System-level overview summarizing the mechanical architecture of the electronics hardware analyzed with key CAD graphics
  - Historical survey of prior analyses (if relevant)
  - Requirements [11]
- Thermal analysis
  - Objective(s)
  - Geometry, which summarizes the thermal/cooling architecture of the electronics hardware analyzed with key thermal model graphics
  - Methodology, including control volume assumptions, thermophysical material properties, boundary conditions, modes of heat transfer accounted for in the analysis, numerical solver settings, and mesh parameters/resolution
  - Results in tabular and graphical formats, including temperatures of electronic components and boards contours (temperature, velocity, pressure)
- Conclusions, including any recommendations and pending or future work
- Backup content, including data reference sources, numerical convergence plots, and any ancillary information relevant to the analysis

The above outline is not intended to be a strict, comprehensive template but rather a guide for what content to include in an analysis report. It excludes necessary sections such as References, Abbreviations, and Appendices. Ideally, all of the above sections include key graphics as figures illustrating the text.

It is difficult to over-document an analysis for most engineers. In fact, most engineers are arguably culpable of under-documenting, owing to the stereotype that engineers prefer numbers and equations over words and prose. Nevertheless, documentation is essential because it retains a detailed historical record of the analysis which will facilitate any future effort recreating the analysis and, more importantly, follow-on efforts expanding on the documented analysis [12]. The more information that is included re-

garding the analyzed system, as trivial or obvious as it may seem, will almost certainly prove useful to subsequent generations of engineers reading the artifact for their analysis tasks.

Best Practice #5: Cost, Schedule, and Scope

Understanding cost, schedule, and scope is critical to performing a successful thermal analysis. Cost refers to the budget of labor hours (units of hours) and material (units of dollars) allotted by the project to perform the thermal analysis; labor hours are ultimately converted into dollars via the engineer's fully-burdened labor rate (i.e., what the company pays for you, including overhead costs). Schedule refers to the time duration and deadline set by the project to perform the thermal analysis; a schedule is monetized into pseudo-dollars by setting a timeline of expected tasks' durations and completion dates. Work scope encompasses the requirements and analysis objectives outlined in the statement of work (formal or informal) for the thermal analysis [11].

It is good practice to clearly understand and adhere to these 3 elements while performing the thermal analysis and for the thermal engineer to pace him/herself accordingly. For example, if a project only has a small budget of 40 labor hours and short schedule of 2 weeks available to perform a new analysis, then the thermal engineer can outline how much (or little) thermal analysis that will buy the project—perhaps spreadsheet-level calculations and a simple conduction model, or updates to an existing model, with a short slide deck for documentation. In contrast, if a project has a large budget of 960 labor hours over a long schedule of 6 months—effectively translating to full-time support over the 6-month timeline—then the thermal engineer can provide a detailed, comprehensive, system- and subsystem-level CFD analysis with a thoroughly documented written report. If an analysis is projected to overrun on cost or schedule, early communication to project management can oftentimes buy the engineer an increase in cost or schedule. Communication is critical. Additionally, (1) "scope creep," i.e., the increase of work scope over time, without a corresponding increase in cost and schedule, and (2) "requirements swirl," i.e., changing requirements over time, which may be due to under-defined or non-firm requirements, each have the potential to financially sink an entire project.

For most of us engineers, it is important to remain cognizant of the fact that we are employed by for-profit organizations. Therefore, maintaining cost and schedule constraints while performing assigned analysis tasks is critical for the company's success. As a for-profit organization, cost and schedule are important metrics that are vital to the company's financial performance and should not be disregarded by the engineer. The thermal engineer has the responsibility of ensuring technical accuracy and soundness in the analysis while adhering to cost, schedule, and scope constraints, which is not a trivial task.

Conclusion

This manuscript outlined five best practices in thermal analysis methodology:

(1) Understanding the relevant fundamental physics;
(2) Having a peer review of the analysis by an experienced, senior engineer;
(3) Performing sanity checks to verify the accuracy of a computational simulation, along with collecting test data to validate the model;
(4) Documenting the analysis clearly and thoroughly;
(5) Adhering to cost, schedule, and scope constraints during the analysis while ensuring technical accuracy.

Following these best practices will promote a successful, well-executed analysis.

Acknowledgements

The author gratefully acknowledges Mr. Greg P. Schaefer, Mr. Dan E. Giles, and Dr. Jim S. Wilson, who have been industry mentors to him at RTX. The author also gratefully acknowledges Dr. Philip S. Schmidt (The University of Texas at Austin) and Dr. Fatemeh Hassanipour (The University of Texas at Dallas), who have been academic mentors to him.

References

[1] Incropera, F. P. et al., Fundamentals of Heat and Mass Transfer, 6th ed., John Wiley & Sons, 2007.
[2] Steinberg, D.S., Cooling Techniques for Electronic Equipment, 2nd ed., John Wiley & Sons, 1991.
[3] Kays, W. M. and London, A.L., Compact Heat Exchangers, 2nd ed., McGraw-Hill, 1964.
[4] Guyer, E.C., Handbook of Applied Thermal Design, 1st ed., Taylor & Francis, 1999.
[5] Marthinuss, J.E., "Air Cooled Compact Heat Exchanger Design For Electronics Cooling," Electronics Cooling, February 2004, https://www.electronics-cooling.com/2004/02/air-cooled-compact-heat-exchanger-design-for-electronics-cooling/
[6] Lindeburg, M.R., Mechanical Engineering Reference Manual (MERM), 13th ed., Professional Publications, 2013.
[7] Kordyban, T., Hot Air Rises and Heat Sinks: Everything You Know About Cooling Electronics is Wrong, 1st ed., The American Society of Mechanical Engineers (ASME), 1998
[8] Electronics Cooling Editorial Board, "Thermal Facts & Fairy Tales: 7 years of college down the drain…," Electronics Cooling, January 2017, https://www.electronics-cooling.com/2017/01/thermal-facts-fairy-tales-7-years-college-drain/
[9] Wilson, J., "Providing More Value Than Playing Video Games," Electronics Cooling, November 2007, https://www.electronics-cooling.com/2007/11/providing-more-value-than-playing-video-games/

[10] Mohammed, R., "Experimental Methodologies for Thermal Design in Silicon Validation Platforms," Electronics Cooling, July 2010, https://www.electronics-cooling.com/2010/07/experimental-methodologies-for-thermal-design-in-silicon-validation-platforms/
[11] Wilson, J., "Thermal Facts and Fairy Tales: Understanding and Defining Electronics Cooling Requirements," Electronics Cooling, July 2016, https://www.electronics-cooling.com/2016/07/thermal-facts-and-fairy-tales-understanding-and-defining-electronics-cooling-requirements/
[12] Wilson, J., "Editorial: Archival Value," Electronics Cooling, March 2011, https://www.electronics-cooling.com/2011/03/archival-value/


Call for Authors
and Contributors!
Want to be a part of the next issue of Electronics Cooling? Have an article or blog post you'd like to write for Electronics-Cooling.com?
Let us know at
editor@electronics-cooling.com
electronics COOLING
www.Electronics-Cooling.com

Index of ADVERTISERS

Electronics Cooling
716 Dekalb Pike, #351
Blue Bell, PA 19422

t: (484) 688-0300
e: info@electronics-cooling.com
w: www.electronics-cooling.com
page: 29

Lectrix
716 Dekalb Pike, #351
Blue Bell, PA 19422

t: (484) 688-0300
e: info@lectrixgroup.com
w: www.lectrixgroup.com
page: 31


Break the same old pattern.
Problem First. Product Last.
Content | Data | Marketing Technology
LECTRIX®
Digital Marketing for the B2B Electronics Industry
1.484.688.0300 | info@lectrixgroup.com
www.lectrixgroup.com